4H-SiC VDMOS – drift-region saturation, channel saturation and their order of appearance

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4H-SiC VDMOS is a peculiar semiconductor structure with two considerably different recognized regions. One of them is a vertical drift region, whereas the other one appears as a horizontal channel with its left and right sections corresponding to source bias. In each of these regions current-voltage characterisic can become saturated regardless of the status of the other region, thus making possible several operation modes of the considered devices. The investigation of the onset of these saturations in their order of appearance is the goal of this paper.

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1. Introduction

In the last decade of the previous century, silicon based devices have reached their technical limits, that opened the question of a new material convenient enough to replace silicon. As a natural successor silicon-carbide (SiC), mostly in the form of 4H-SiC or 6H-SiC, has emerged giving new life to the corresponding structures. Compared to silicon ones, the silicon-carbide devices [e. g. 1 – 3] are able to operate under harsher conditions, that becomes unavoidable for use in hybrid electric vehicles (HEV), geological equipment or military industry. Among numerous advantages, some of them are worth mentioning:

- SiC devices can operate at very high temperatures; the temperature of 600^0C has been reported in the literature, while Si ones maintain their reliability only up to 150^0C;
- SiC devices have lower switching losses and therefore they are expected to operate even at very high frequencies (10 – 100GHz) and so surpass Si based ones ten times [4];
- the critical electric field in silicon-carbide is ten times higher than the critical electric field in silicon, permitting this way a hundred times higher doping concentration for the same breakdown voltage to be reached (it also means that for the same doping level, silicon-carbide devices have at least ten times higher breakdown voltage) [5 - 7];
- last but not least, silicon-carbide unipolar devices are thinner and have considerably lower on-resistances (approximately hundred times less than their silicon counterparts).

That is not the end of the list, but even already mentioned advantages announce silicon-carbide as a promising candidate whose investigation makes sense. It is also fair to say that silicon-carbide devices have some disadvantages, but we have enough courage to claim that the most of these disadvantages (or shortcomings as well) stem from the immature or insufficiently developed processes of producing corresponding devices [5].

2. General features of the VDMOS structure

A structure considered in this paper (VDMOS - Vertical Diffused Metal Oxide Semiconductor) is shown in Fig. 1 [1]. Its crucial component (not met in the convenient MOS structure) is a vertical drift region. It begins with a narrow section embedded in p-body substrate (section A) occupied by a constant vertical drain current I_D in the above direction. The region of greater width is positioned beneath region A and three important sections can be recognized in it: just beneath p-body layers two sections arise (left and right) which are supposed not to be occupied by drain current; between them, the section B is embedded – its width steeply increases in downward direction and it is occupied by drain current; just above drain bias and beneath B section region C of constant and as great as possible width exists (occupied by drain current again). The drift region is supposed to be lightly n-doped and fully ionized [2, 3].

The heavily doped n^+-regions beneath source bias and encircled by p-bodies are connected with A-section of a vertical drift region by horizontal channels (left and right) occupied by drain current and so providing the global continuity equation to be satisfied. These channels are rather short (~1μm) and their modeling must be carefully performed.

The described structure (denoted as VDMOS) has been proposed and developed in order to meet several requirements. The presence of silicon-carbide instead of silicon results in considerably higher values of breakdown

voltage**,** what plays an important role in the channel region. On the other side, drift region can sustain very high voltage drops; these two facts can provide large drain currents, what together with high voltage makes this structure convenient for use in power electronics.

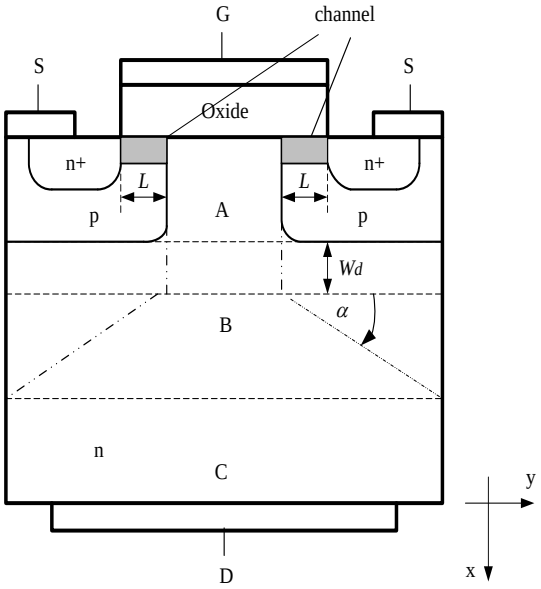

Fig. 1. VDMOS structure used for investigation and modeling in this paper with different regions of operation labeled.

The channel region and the drift region can be investigated and modeled almost separately; the common quantity for both regions is drain current, while drain-to-source voltage is a sum of voltage drops across drift region and one of the channels [6]:

$$V_{DS} = V_{drift} + V_{ch} \tag{1}$$

The channel region is nothing else but the convenient MOS structure in details investigated and modeled in the literature. In this paper, the following approximate form to describe current-voltage characteristic has been adopted [8, 9]:

$$I_{D,ch} = \mu_n^* \cdot \frac{W}{L} \cdot C_{ox}' \cdot \frac{2\left(V_{GS} - V_T\right) \cdot V_{ch} - \left(1+\delta\right) \cdot V_{ch}^{\,2}}{1 + \frac{\mu_n^*}{L \cdot v_s^*} \cdot \frac{V_{GS} - V_T}{1+\delta}}$$

$$V_{ch} \le V_{GS} - V_T \tag{2a}$$

$$I_{D,ch}^{\,SAT} = \mu_n^* \cdot \frac{W}{L} \cdot C_{ox}' \cdot \frac{\frac{\left(V_{GS} - V_T\right)^2}{1+\delta}}{1 + \frac{\mu_n^*}{L \cdot v_s^*} \cdot \frac{V_{GS} - V_T}{1+\delta}}$$

$$V_{ch} \ge V_{GS} - V_T \tag{2b}$$

where W and L are channel width and length respectively, while C_{ox}' denotes the oxide layer capacitance per unit area. It is worth mentioning that surface mobility μ_n^* and surface saturated velocity v_s^* are considerably smaller compared to corresponding bulk values (for practical conditions and lightly doped substrates the surface mobility is roughly half of the bulk mobility). The zero-order estimate for correction coefficient δ (sufficient for rough calculations) is accepted as follows [9, 10]:

$$\delta = \frac{\gamma}{4\sqrt{2\Phi_F}} = \frac{\frac{\sqrt{2\varepsilon N_A \in_S}}{C_{ox}'}}{4\sqrt{2\Phi_t \ln\left(\frac{N_A}{n_i}\right)}} \tag{3}$$

In equation (3) N_A is the doping level of p-bodies, Φ_t thermal voltage, n_i the intrinsic concentration and Φ_F the Fermi level. The short channel effects have been accounted for exploiting velocity saturation concept, making this model reliable enough. For the sake of this paper, only the saturated drain current (2b) will play an important role.

As already mentioned, the conducting part of drift region can be divided into three sections (A, B, C). Transport properties of drift region are assumed not to be different from the bulk case. In the frame of drift-diffusion model, transport is adequately described by the (bulk) low field mobility μ_n and saturation velocity (in the bulk again) v_s.

The shape of transport characteristic reliable enough for the purpose of this paper is given by:

$$v = \frac{\mu_n \cdot \frac{dV}{dx}}{1 + \frac{\mu_n}{v_s} \cdot \frac{dV}{dx}}, \quad j = e \cdot n \cdot v \tag{4}$$

where j labels current density (current per unit area). Obviously, for the accumulation section A of drift region (cross-section WL_d, geometric quantities labeled in Fig. 1), the drain current becomes:

$$I_D = eWN_D\mu_n L_d \cdot \frac{\left|\frac{dV}{dx}\right|}{1 + \frac{\mu_n}{v_s} \cdot \left|\frac{dV}{dx}\right|} \tag{5}$$

The extraction of $\left|\frac{dV}{dx}\right|$ out of relation (5) and its integration over accumulation section length W_A simply gives the corresponding voltage drop V_A [6]:

$$V_A = \frac{I_D W_A}{eWN_D\mu_n L_d - \frac{\mu_n}{v_s} I_D} = \frac{I_D\left(W_J + W_d\right)}{eWN_D\mu_n L_d - \frac{\mu_n}{v_s} I_D} \quad (6)$$

It is worth mentioning that the accumulation layer turns out to be as short as possible, i.e. the region between p-bodies with depletion width added, being in perfect agreement with basic principles of physics.

The section B is assumed to have uniformly changing cross-section. Similarly to the relation (5), the expression for drain current becomes ($W_A \le x \le W_A + 0.5 L_p \mathrm{tg}\alpha$) [9 - 11]:

$$I_D = \frac{eWN_D\mu_n\left[L_d + 2\left(x - W_A\right)ctg\alpha\right]\cdot\left|\frac{dV}{dx}\right|}{1 + \frac{\mu_n}{v_s}\cdot\left|\frac{dV}{dx}\right|} \quad (7)$$

or

$$\left|\frac{dV}{dx}\right| = \frac{I_D}{eWN_D\mu_n\left[L_d + 2\left(x - W_A\right)\cdot ctg\alpha\right] - \frac{\mu_n}{v_s} I_D} \quad (7a)$$

$$V_B = \frac{I_D}{2eWN_D\mu_n ctg\alpha}\cdot \ln\frac{eWN_D\mu_n\left(L_d + L_p\right) - \frac{\mu_n}{v_s} I_D}{eWN_D\mu_n L_d - \frac{\mu_n}{v_s} I_D} \quad (8)$$

The parameter α (tgα) can also be estimated from the basic principles. Rough calculations sufficient for the purpose of this paper suggest its value very close to tgα=1 [9].

The carrier transport in section C is rather similar to that in section A, but with the increased cross-section. Therefore the expression for the corresponding voltage drop can be written straightforward:

$$V_C = \frac{I_D\left(W_T - W_J - W_d - \frac{1}{2}L_p tg\alpha\right)}{eWN_D\mu_n\left(L_d + L_p\right) - \frac{\mu_n}{v_s} I_D} \quad (9)$$

where $\left(W_T - W_J - W_d - \frac{1}{2}L_p tg\alpha\right)$ clearly denotes the C section height (vertical dimension). The entire voltage drop over the whole drift region now becomes:

$$V_{DRIFT} = V_A + V_B + V_C \quad (10)$$

that together with the relation (1) gives drain-to-source voltage V_{DS} unavoidable in constructing usual current voltage characteristic $I_D(V_{DS})$. There are several developed procedures of doing it, but the focus of this paper is something else. Obviously, the relations (6) and (8) result in very big values of voltage drops V_A, V_B (tending to infinity) for some specific values of drain current. In other words, the drain current limit exists and can not be exceeded for arbitrary high values of drift region voltage. This effect reminds of saturation very much, hence it will be called drift-region saturation and the described maximal drain current becomes [1, 2]:

$$I_{Do} = eWN_D L_d v_s \quad (11)$$

when the denominator of (6) turns to zero.

On the other hand, drain current in horizontal channels also has its upper limit defined by the expression (2b). While none of these values can be exceeded, the conclusion will be rewritten in an elegant form:

$$I_D{}^{SAT} = \min\left(I_D{}^{ch,SAT}, I_{DO}\right) \quad (12)$$

Expression (11) implies that drift-region saturation drain current is controlled through the doping level of drift region, together with the tuning of geometric parameters W, L_d. The channel saturation itself is controlled through the change of gate voltage V_{GS}, accompanied by the design of geometric parameters W, L, t_{ox} etc. The expression (12) is conveniently illustrated in Fig. 2. The almost linear dependence of channel-saturation drain current on V_{GS} (except for its very small values) gives a proof that the quasi-saturation really takes place, as expected in high voltage power devices [13].

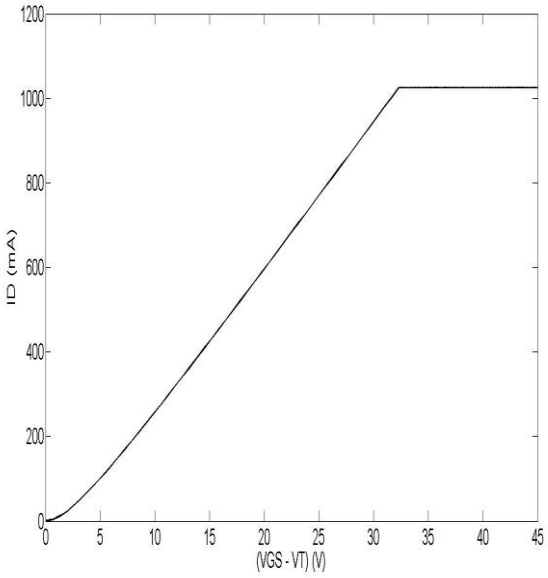

Fig. 2. The cumulative saturation drain current $I_D{}^{SAT}$ versus gate voltage V_{GS}.

It is also worth noticing that we are unable to reach the drain current values arbitrary close to I_{DO}. The breakdown electric field EB sets a strict border for it which is efficiently 1% smaller than $I_D^{q,SAT}$:

$$I_{DOeff} = I_{DO} \cdot \frac{E_B}{\frac{v_s}{\mu_n} + E_B} \tag{13}$$

This fact also imposes a strict theoretical limit for V_{DRIFT}:

$$\begin{aligned} V_{DRIFT} \le E_B W_A + \frac{v_s L_d}{2\mu_n} tg\alpha \cdot \ln\left(\frac{L_p}{L_d} \cdot \frac{E_B \mu_n}{v_s}\right) + \\ + \frac{v_s}{\mu_n} \cdot \frac{L_d}{L_p} \cdot \left(W_T - W_A - \frac{1}{2} L_p \cdot tg\alpha\right) = V^B{}_{DRIFT} \end{aligned} \tag{14}$$

For the sake of this paper's goal, the drift region voltage drop will be rewritten in a more transparent form obtained by inserting relation (11) into expression (10):

$$\begin{aligned} V_{DRIFT} = \frac{v_s}{\mu_n} \cdot W_A \cdot \frac{I_D}{I_{DO} - I_D} + \\ + \frac{v_s}{\mu_n} \cdot \frac{L_d tg\alpha}{2} \cdot \frac{I_D}{I^{q,SAT}} \cdot \ln \frac{\left(1 + \frac{L_d}{L_p}\right) I_{DO} - I_D}{I_{DO} - I_D} + \\ + \frac{v_s}{\mu_n} \cdot \left(W_T - W_A - \frac{1}{2} L_p tg\alpha\right) \cdot \\ \cdot \frac{I_D}{\left(1 + \frac{L_p}{L_d}\right) I_{DO} - I_D} \end{aligned} \tag{15}$$

Obviously, drift region voltage drop becomes rather simple and for further analysis convenient function of the ratio I_D / I_{DO} that will be thoroughly exploited in the next section.

3. Numerical simulation and discussion

The model derived in this paper has been tested for a specific set of geometric and technological parameters describing the investigated structure [3, 6]:

W=400μm W_J=30μm N_D=$4\cdot10^{21}$m^{-3}

L=1μm W_d=2μm N_A=$4\cdot10^{23}$m^{-3}

v_s=$2\cdot10^5$m/s L_d=20μm t_{ox}=50nm

μ_n=0.08m2/Vs L_p=50μm W_T=70μm E_B=$2.2\cdot10^8$V/m

The results of this simulation are shown in Fig. 3. The shape of the characteristic agrees with expectations and deserves some additional comments necessary for the correct understanding of device's operation and the requests standing in front of it.

The region of small drain currents and small drift region voltages (I_D≤400mA, V_{DR}≤100V for a chosen set of technological and geometric parameters) can be recognized as linear regime. Drift region voltage drop is proportional to drain current with a calculable resistance value. The operation of such device is entirely governed by the phenomena taking place in the channel, while drift region behaves just as an ohmic resistor added in a series to the pair of conventional MOSFETs. To this regime no further attention should be paid, i.e. such device could not meet the specific requests for VDMOS design and application. The regime corresponds to V_{GS} voltages not greater than 15V.

The next region observed in Fig. 3 will be denoted as nonlinear regime (approximately 400mA≤I_D≤750mA and 100V≤V_{DR}≤400V, corresponding values of V_{GS} lying between 15V and 25V). The departure of the characteristic from linear regime toward saturation is obvious, while the achieved values of drain current and consequently calculated drift region voltages start meeting the requests of application in power electronics. The regime is believed to have considerable importance.

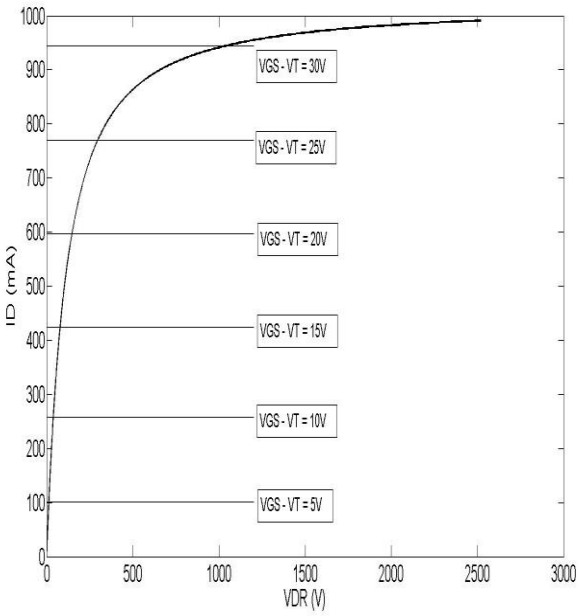

Fig. 3. Drain current versus drift region voltage drop.

The most interesting region arising from Fig. 3 is the strongly nonlinear sub drift-region saturation regime. Its most important features are relatively narrow range of drain current values (750mA≤I_D≤I_{DOeff}) accompanied by a wide range of drift region voltage values (V_{DR}≥400V). It is necessary to say that the drift region voltage drop

corresponding to the achievement of breakdown electric field lies too high (~7kV) and never occurs. For practical purposes, one can assume that device operation becomes seriously disturbed, i.e. the developed model becomes questionable at the moment when the depleted region is spread as much as possible beneath n+ region. In this case, C region (Fig. 1) disappears, while A region reaches its maximal value and region B survives. For the chosen set of geometric and technological parameters, this happens for drift region voltage drop of approximately 2.5kV. Last but not least, the sub-saturation regime requires gate-to-source voltage V_{GS} to be above 25V ($V_{GS}\geq$25V).

The channel itself must also be kept safe from breakdown. The conventional MOSFET theory neglects horizontal (lateral) electric field in comparison to the vertical one and the constraint that vertical electric field must not exceed breakdown electric field E_B sets the upper limit for gate-to-source voltage at about 45V (V_{GS}<45V).

The power electronics application demands relatively high values of drain current I_D and drain-to-source voltage V_{DS} (whose biggest part is accompanied to the drift region), what recommends the nonlinear regime and especially sub-drift region saturation regime as operation regimes of the greatest interest. The limiting fact concerning these regimes safe from breakdown is a rather narrow "gap" of gate voltages providing it (20V≤V_{GS}≤35V). As the upper limit is fixed, the only way to alleviate this problem is to somehow reduce the lower limit (adjusting geometric and technological parameters in the allowed range or designing a similar structure with considerably improved features).

6. Conclusion

In this paper the impact of drift-saturation (and hence the value of drift-saturation drain current) has been studied in details. Although drift-saturation is never achieved, it has been analytically shown and by simulations confirmed that it played very important role even for smaller values of drain current. On the other hand, rather big values of drift voltage and drain current appearing in our calculations should not worry; they were the consequence of rather big values of geometric parameters accepted in this paper. Further size reduction will indispensably lead to lower values of drift region voltage drop and drain current, at first place of drift region saturation current, but the general shape of obtained dependances will be sustained.

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