A new topology of converter fed multilevel inverter for medium to high power applications

S. MALATHI*, S. CHANDRAMOHAN[a]
Research Scholar, Department of Electrical and Electronic Engineering, Anna University, Chennai, India
[a]Associate Professor, Dept of Electrical and Electronics Engg, College of Engineering, Anna university, Chennai, India

This paper proposes a novel PFC Boost converter fed multilevel inverter topology. Conventional bridge PFC Boost converter has high conduction losses in the input rectifier bridge and it gives poor power factor. High efficiency and UPF (unity power factor) can be achieved by this proposed closed loop controlled Bridgeless PFC Boost converter. This converter unit is fed to a new cascaded H-bridge seven-level inverter which has less number of switches and voltage sources compared to the existing inverters like diode clamped, flying capacitors and cascaded multilevel inverters. Therefore, the overall cost has greatly reduced. The term staircase modulation technique is used to control the proposed inverter. This control method tends to generate a staircase voltage. The proposed topology gives less Total Harmonic Distortion (THD) and high power output. So it can be used in high power applications like Marine and Industrial applications. Simulation work is carried out by using MATLAB/SIMULINK. Finally, a prototype of the proposed converter fed seven-level inverter topology is built and tested to show the performance and high output voltage of the converter fed inverter by experimental results.

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Keywords: Level generation unit, Polarity generation unit, Staircase modulation, Power Factor Correction, Unity power factor, Total Harmonic Distortion

1. Introduction

Recent years, the non-linear loads such as UPS, rectifiers, arc furnaces, computers, electric drills, industrial electronic equipment consists of power semiconductor devices such as thyristor Inverters and converters) are becoming major part of the electrical load in commercial and industrial power system. Suchkinds of loads draw non- sinusoidal currents from the input power supply and it will lead to voltage harmonic distortion and simultaneously it will affect the PF (power factor). To increase the PF (power factor) of AC side,PFC (power factor correction) boost converters are generally used. Such converters are used to adjustthe input current waveform to sine (sinusoidal) waveform [1], [2]. In general,various topologies used in PFC (Power Factor Correction) converters, such as buck, boost,fly back and interleaved.Performance comparison between Bridge-PFC boost converter (conventional) and bridgeless PFC boost converter is mentioned in [3]. Bridgeless PFC boost converter has less CM (Common Mode) noise and also it has less voltage drop. So its power factor is high (nearer to unity) [4].

ZVS (Zero Voltage Switching) interleaved boost converter is one of the power factor correction converter which is ac to dc converter. It is used to charge the battery of an EV (Electric Vehicle) from the utility mains [5], [6]. It consists of two parts. One is front-end boost converter (performs ac/dc conversion and input PFC), and fullbridge dc/dc converter (galvanic isolation and battery charging).Multi-level Inverters (MLI)are another important research area in power electronics. In Multilevel inverters have received more advantages because of their high efficiency, high voltage operation and low EMI (electromagnetic interference) [7].MLIs are applicable for medium to high voltages and high power applications [8], [9].NPC (Neutral-Point Clamped), FC (Flying-Capacitor) and CHB (Cascaded H-Bridge) inverter topologies are most commonly used multilevel inverter structures [10]. Compared to FC and NPC MLI topologies CHB MLI is easy to design. Since it uses less number of IGBT switches. Two common topologies for CHB inverters are symmetric and asymmetric structure [11]. Symmetric (all the voltage sources are equal) cascaded H-Bridge inverter uses more number of switches and the asymmetrical (voltage sources are unequal) CHB topology uses less number of switches but gives more output voltage levels.A new topology of Reverse Voltage (RV MLI) multilevel inverter with reduced number of switches, voltage sources and insulated gate driver circuit has been implemented and presented in [12],[13]. This multilevel inverter topology is controlled by PDPWM (Positive Disposition Pulse Width Modulation) control strategy.

A generalized cascaded H-bridge multi-level inverter by using sub multi-level inverter (connected in the form series) is mentioned in [14]-[17]. Each sub MLI has two switches. Sub MLIs are connected to H-bridge inverter which has four switches. Sub MLIs are used to generate output voltage with required levels and the H-bridge MLI is used to give output stepped voltage with positive or negative polarity. Compared to the above mentioned topologies, this MLI uses less number of voltage sources

and switches. Apart from these, this paper proposes a new topology of converter fed inverter which is used in medium to high power applications. Proposed closed loop controlled power factor correction boost converter uses only two switches and diodes but it gives unity power factor at the supply side. So output voltage and efficiency of the converter has greatly increased. Proposed MLI is seven-level asymmetrical structure which has only eight switches and two dc voltage sources but it will generate seven-level output.Compared to carrier based PWM control strategies staircase PWM technique produces less THD [18], [19]. So staircase modulation control technique (constant frequency modulation strategy) is used to control the proposed MLI. This modulation strategy is constant frequency modulation control technique which does not require any carrier and gate signals[20]. So the complexity of the circuit has particularly for higher output voltage levels. By using this proposed bridgeless PFC boost converter output voltage and the performance of the MLI has greatly increased.

2. Block diagram of proposed topology

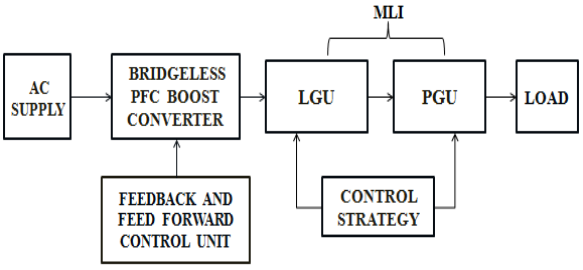

Fig. 1. Block diagram of proposed converter fed inverter.

Fig.1 shows Block diagram of closed loop controlled Bridgeless PFC Boost converter fed inverter. In this, ac supply is given to Bridgeless PFC Boost converter. Feed forward and feedback control unit is fed to this converter. By using this control unit power factor is increased to unity. Output of the Bridgeless PFC Boost converter is fed to a new seven-level generalized H-bridge multilevel inverter. Proposed MLI has two units i.e. LGU (Level Generation Unit), PGU (Polarity Generation Unit). LGU is used to generate output voltage with required level. PGU is used to produce output voltage with positive or negative polarity. Staircase PWM technology is used to control the multilevel inverter.

3. Circuitdiagramofproposed topology

Fig.2 shows circuit diagram of closed loop controlled Bridgeless PFC Boost converter fed a new generalized H-bridge multilevel inverter. The main aim of this topology is to produce high level ac output voltage by using lower lever ac input voltage. Proposed topology is divided into two sections. One is converter section and the other one is inverter section. PFC Boost Converter section consists of ac input voltage source V_{in}, inductor L_1, diodes (D_A and D_B), IGBT Switches (S_A and S_B) and capacitor $C_{o.}$. Control unit of the converter section produces switching signals to IGBT switches S_A and S_B. Multilevel inverter section has eight switches. Switches S1, S2, S3 and S4 are used to generate required output voltage levels without polarity. Switches S5 and S6 are used to produce positive half cycle output voltage. Switches S7 and S8 are used to produce negative polarity output voltage. Staircase modulation control techniqueis used to control the inverter section switches (S_1 to S_8) which minimize Total Harmonic Distortion (THD).

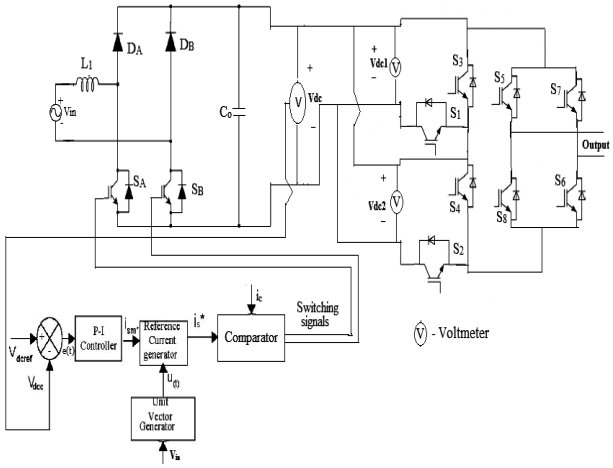

Fig. 2. Circuit diagram of converter fed proposed MLI.

Proposed multilevel inverter is seven-level asymmetrical topology which requires less number of switches and voltage sources. Therefore, the overall cost and complexity are greatly reduced. This topology gives less Total Harmonic Distortion (THD) and high output voltage. Switching sequences for proposed seven-level asymmetrical multilevel inverter is shown in Table 1.

Table 1. Switching sequences for proposed MLI.

S1	S2	S3	S4	S5	S6	S7	S8	Vo
1	1	0	0	1	1	0	0	Vdc1+Vdc2
0	1	1	0	1	1	0	0	Vdc2
1	0	0	1	1	1	0	0	Vdc1
0	0	1	1	1	1	0	0	0Vdc
1	0	0	1	0	0	1	1	-Vdc1
0	1	1	0	0	0	1	1	-Vdc2
1	1	0	0	0	0	1	1	-(Vdc+Vdc2)

4. Operations of proposed MLI

Fig.3 indicates levels of operation of proposed seven-level multilevel inverter. Red line indicates the current flow direction. There are seven levels of operations are possible for seven-level proposed MLI. Switches 5 and 6 will conduct for first four levels and give positive polarity

output. Switches 7 and 8 will conduct for next three levels and give negative polarity output.

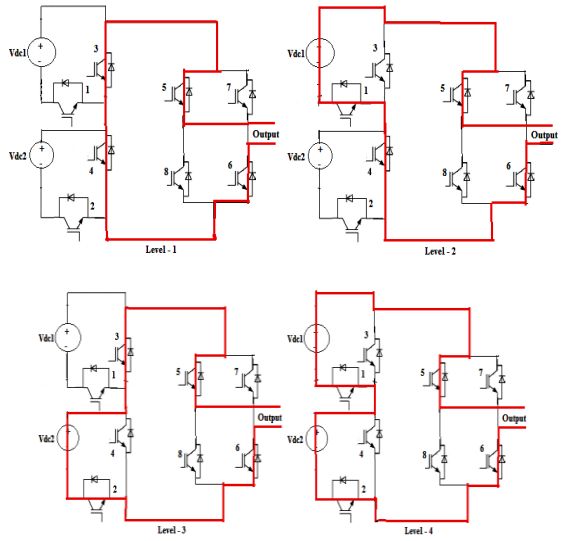

Fig. 3. Operation of proposed seven-level asymmetrical multilevel inverter.

5. Formulasforproposed inverter

Number of maximum output voltage levels

$$N_{levels} = 2\,(k+1)^m - 1 \quad (1)$$

Number of switches required is,

$$N_{switches} = 2mk + 4 \quad (2)$$

Number of dc voltage sources used is,

$$N_{dc\ sources} = m*k \quad (3)$$

Where,
m- Number of cascaded submultilevel inverters in LGU
k- Number of cascaded H-Bridge inverter in PGU

The maximum output voltage of the proposed multilevel inverter is:

$$V_{omax} = k \sum_{j=1}^{m} Vdc, j \quad (j=1, 2, 3\ldots..m) \quad (4)$$

$$V_{dc,1} = V_{dc1} \quad (5)$$

$$V_{dc,2} = (k+1)\, V_{dc2} \quad (6)$$

$$V_{dc,3} = (k+1)^2\, V_{dc3} \quad (7)$$

For seven level, m=2 and k=1 for all the cases then
$N_{levels} = 7$, $N_{switches} = 8$

$$V_{omax} = Vdc1 + 2\,Vdc2 \quad (8)$$

V_{dc1}- dc voltage source of the first submultilevel inverter
V_{dc2}- dc voltage source of the second submultilevel inverter

6. Simulationresults

In this section, the simulation result of the proposed converter fed inverter topology is presented. These results are carried out by using Matlab/Simulink. The value of boost up inductor is 1mH and the capacitor used in the converter side is 470 µF.The inverter output is connected to a single phase R-L load. The value of R is 50 ohm and L is 182mH.

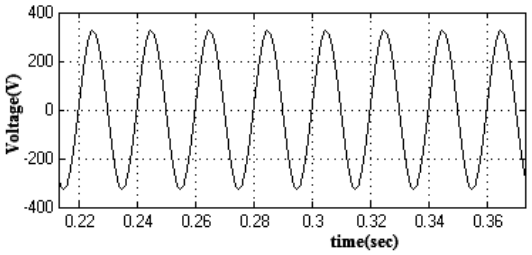

Fig. 4. Input Voltage waveform of the converter.

Input RMS voltage of the converter is 230V ac i.e. 325V peak to peak which is shown in Fig. 4.

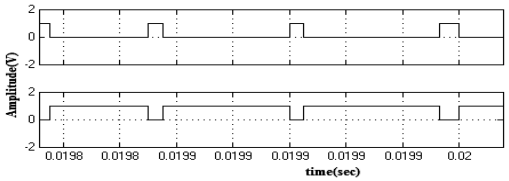

Fig. 5. Pulses given to switches.

Pulses produced by closed loop control unit are shown in Fig. 5 which is given to switches S_A and S_B.

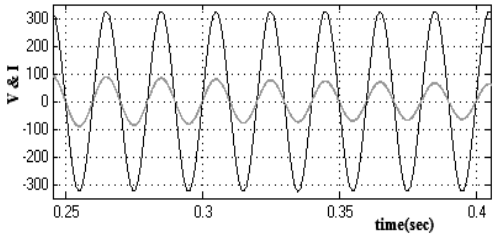

Fig. 6. Unity Power Factor at the supply.

Fig. 6 shows the input voltage and current waveform of proposed converter which are in phase. So the power factor is unity.

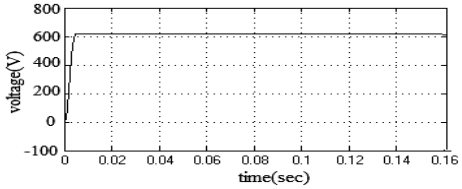

Fig. 7. Output Voltage of proposed converter.

Output voltage of the proposed converter is 602V DC output which is shown in Fig. 7.

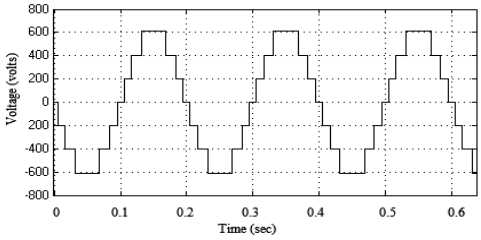

Fig. 8. Seven-level inverter output voltage waveform.

The proposed inverter topology is used to generate seven-level stepped output voltage for a resistive and inductive load. The seven-level inverter stepped output voltage waveform is shown in Fig. 8 and the corresponding harmonic spectrum is shown in Fig. 9. The output voltage of the inverter is 610 V.

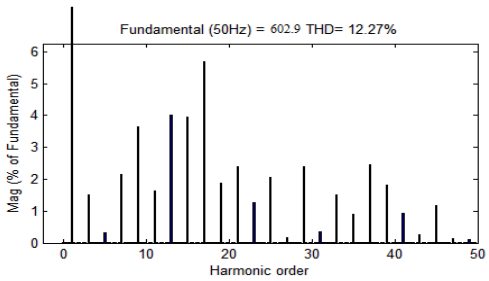

Fig. 9. Output Voltage THD.

Output Voltage Harmonic Distortion is 12.27% and the fundamental is 602.9 peak to peak.

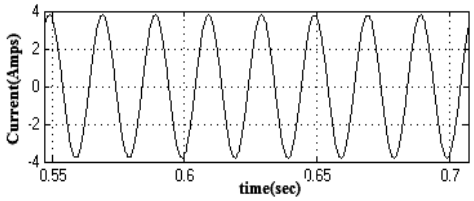

Fig. 10. Output current waveform.

Output current waveform of the proposed MLI is shown in Fig.10 and the corresponding Harmonic spectrum is shown in Fig. 11. Output current is 3.9A and the corresponding Harmonic spectrum is 0.82%.

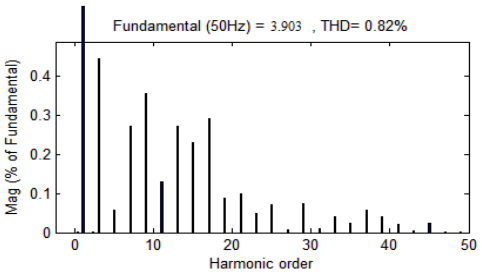

Fig. 11. Current Harmonic spectrum.

7. Hardware Implementation

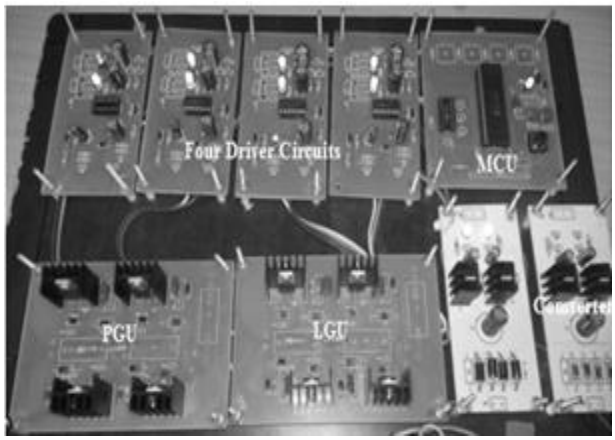

Fig. 12. Hardware Implementation of proposed converter fed inverter topology.

Experimental prototype for proposed converter fed seven-level inverter topology is shown in Fig. 12. It consists of regulators, converter unit, inverter (level and polarity generation units), four driver circuits and micro controller units. IRF840 MOSFET is used in both converter and inverter units. Each MOSFET are driven by driver circuits. IR2112 driver IC is used in driver circuits.The PWM controller is implemented by PIC16F877A microcontroller.Since its response time is faster and its size is small. The 5V regulator (LM7805) is used to give supply to the micro controller unit and the 12V regulator (LM7812) is used to give supply to the four driver circuits. Diodes (1N4000 and 1N5408) and capacitor (470 µF) are used in converter section. In this ac supply used is 230V ac which is givento PFC Boost converter section. Output voltage of the PFC Boost converter is 605V dc which is given to inverter section. It is used to convert 605V dc to 605V ac. i.e. this proposed converter fed inverter topology is used to generate seven voltage levels for a resistive (R=50ohm) and inductive load (L=182mH). The experimental output voltage is $605V_{P-P}$.

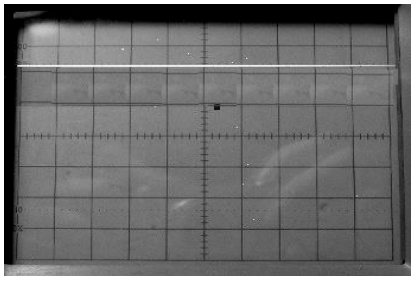

Fig. 13. Converter output voltage (scale 300V/div), time scale (5ms/div).

Fig. 13 shows the output voltage at PFC Boost converter side. Output voltage of the converter is 605V dc.

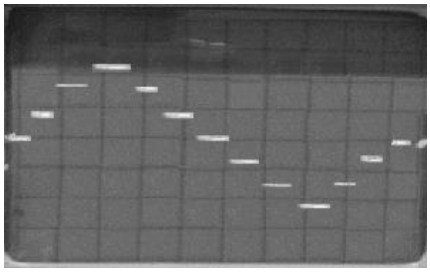

Fig. 14. Inverter output voltage (scale 300V/div), time scale (5ms/div).

Fig. 14 shows the seven-level stepped output voltage at inverter side. Output voltage of the inverter is 605V ac. By using 230V ac input voltage, this topology can generate 605V ac output voltage. So this topology can be used for medium to high power applications.

8. Conclusion

In this paper, a new topology of converter fed inverter has been proposedwhich has more features over existing topologies interms of the required isolated dc supplies and power semiconducting switching devices,control requirements, reliability and cost. It is observed that this topology can be used in powerapplications such as HVDC, FACTS, UPS, PV systems, etc. Inthe mentioned converter fed inverter topology, the switching sequences for inverter is separatedinto low and high frequency parts. This can add up to the performance and efficiency of the topology as well as reducing cost and the size of the experimental prototype.The staircase modulation control method is used to drive the inverter.The Pulse Width Modulation (PWM) for this topology has fewer complexities since it does not require any modulation or carrier signal.The hardware results of the developed prototype for a converter fed seven-level inverter of the proposed topology are demonstratedin this paper and the results are observed. The results clearly indicate that the proposed converter fed inverter structure can effectively work as a converter and multilevel inverter with areduced number of power semiconductor switches.

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*Corresponding author: nmgeswa@gmail.com