An analog circuit design and FPGA-based implementation of the Burke-Shaw chaotic system

ISMAIL KOYUNCU[a,*], AHMET TURAN OZCERIT[b], IHSAN PEHLIVAN[c]
[a]*Control and Automation Technology, Duzce University, 81010, Uzunmustafa, Duzce, Turkey*
[b]*Faculty of Technology, Computer Engineering Department, 54187, Serdivan, Sakarya, Turkey*
[c]*Faculty of Technology, Electrical and Electronics Engineering Department, 54187, Serdivan, Sakarya, Turkey*

In this study, the Burke-Shaw chaotic system has been modeled in three different platforms. In the first stage, the chaotic system has been modeled numerically with the RK5-Butcher algorithm, and the obtained time series and phase portraits are presented. In the second stage, the chaotic system has been modeled with analog circuit components. The results obtained from the numerical modeling confirm the validity of the modeling with analog components. In the final stage, in order to study the RK5-Butcher algorithm, the Burke-Shaw chaotic system has been modeled in VHDL, a hardware description language. The results of the FPGA-based and the numerical modeling results have been compared each other and a sufficient validation score achieved. According to the test results, the operation frequency of the FPGA-based chaotic oscillator is 373.094MHz and it can generate a million-data set in 0.796 seconds.

(Received May 30, 2013; accepted September 18, 2013)

Keywords: Chaos, Chaotic system, FPGA, VHDL, Chaotic generator

1. Introduction

Before it was identified as a scientific phenomenon, the term “chaos” was used to express adverse behavior and situations such as confusion and disorder. The chaos theory was scientifically defined as a concept by Edward Lorenz, who was working as a meteorologist [1]. In his study, Lorenz modeled the air flow in the atmosphere and showed that even very small changes in the outset values can cause great changes in the characteristic behavior of the system. A physical chaotic system similar to Lorenz's system was developed in a laboratory environment for the first time by Chua. The Chua circuit is the most basic chaotic system which has been mathematically proven and is used for chaos formation [2]. The literature includes numerous chaotic systems that have been developed [3-5]. The primary features of these chaotic systems are: being in an internal order and not being random, not repeating previous behavior and consisting of various periodic oscillations in unlimited number, and having a wide power spectrum which includes noise. Additionally, the limit cluster is in a fractal dimension and involves signs, amplitude and frequency which cannot be determined, but change in a limited area. The major feature of chaos and chaotic systems is their sensitive dependence on initial conditions [6]. Due to these characteristics, chaotic systems have been used in widely different branches of science. In particular, they are used a great deal in the engineering sciences [7-9]. In addition, as information security is very important today, chaotic systems are commonly being applied to cryptology and security communication because of their unpredictable features and wide spectrum that includes noise [10-11]. The main difference between chaos-based security communication systems and the traditional ones is the use of chaotic signals instead of sinusoidal signs. According to the literature, chaotic systems have become an alternative to standard wide-spectrum communication systems due to the fact that these systems can encode notice signs simultaneously, and they can carry out such procedures with their low-cost and basic electronic circuit apparatus. On the other hand, chaotic systems are exponentially sensitive to initial values, and it is not possible to anticipate the solution for long time intervals. Because of the above reasons, the interest in chaotic-based broadband communication systems has gradually increased all over the globe. Today, physical modeling and hardware implementation of chaotic systems are needed in many types of scientific research, technological practices, and various other areas particularly cryptology and security communication. The second part of this study is related to the numerical simulation and electronics circuit implementation of the Burke-Shaw chaotic system (BSCS). Moreover, the electronics circuit model has been implemented by individual analog circuit components. In the third part, an FPGA-based model of the Burke-Shaw chaotic system using the RK5-Butcher algorithm is presented. The FPGA-based model has been tested and successful results achieved. The results are evaluated and concluded in the final section.

2. Numerical analysis of the BSCS and electronics circuit implementation

Chaotic systems are generally represented with differential equations or difference equations. The equation system (1) for the Burke-Shaw non-linear

autonomous chaotic system is presented below. In these equations, α and β are system parameters and x, y, and z are dynamic variable of the system. A variation of parameters in the system changes the dynamic behavior of the chaotic system. Thus, the value of these parameters is highly important. In chaotic systems, these critical parameters are referred to as bifurcation parameters. In the current study, α parameter has been determined as *10.0* and β parameter as *13.0*. The initial conditions of the chaotic system are: x_0=*0.6*, y_0=*0.0*, and z_0=*0.0*.

$$\begin{aligned} dx/dt &= -\alpha \cdot x - \alpha \cdot y \\ dy/dt &= -\alpha \cdot x \cdot z - y \\ dz/dt &= \alpha \cdot x \cdot y + \beta \end{aligned} \tag{1}$$

The time series and phase portraits obtained from the modeling are presented in Fig. 1 and Fig. 2 respectively. The BSCS has been modeled numerically with the RK5-Butcher algorithm in order to verify the results of the electronics circuit design.

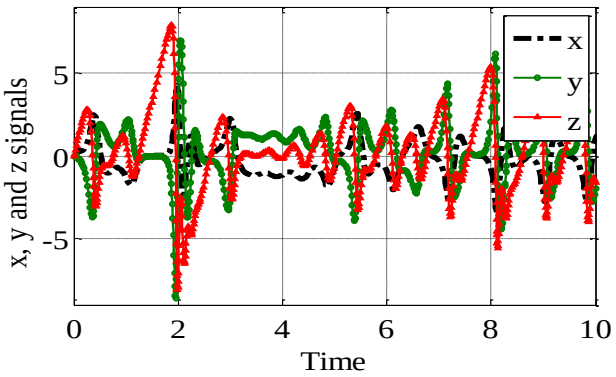

Fig. 1. x, y, and z time series diagram of BSCS.

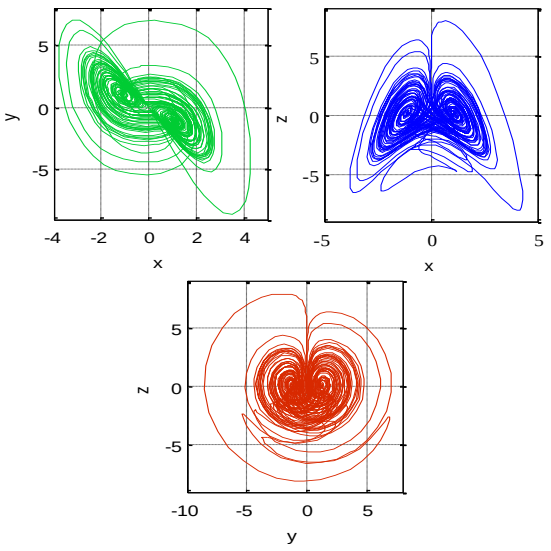

Fig. 2. Results of numerical modeling: (a) x-y phase portrait (b) x-z phase portrait (c) y-z phase portrait.

As seen in Fig.2, the top and bottom offset values of x, y and z signals vary between the range of -7 V and 6 V. The BSCS ranks among the supply values of the op-amp supplied with *±15 V*. Thus, there is no need for any scaling to design the chaotic system with individual electronics circuit components. When the Burke-Shaw chaotic system is modeled with analog electronic components, following differential equations (2) are used.

$$\begin{aligned} dx/dt &= -\left(\frac{1}{R_3C_1}\right)\cdot x - \left(\frac{1}{R_1C_1}\right)\cdot y \\ dy/dt &= -\left(\frac{1}{R_2C_2}\right)\cdot x\cdot z - \left(\frac{1}{R_2C_2}\right)\cdot y \\ dz/dt &= \left(\frac{1}{R_7C_3}\right)\cdot x\cdot y + \left(\frac{1}{R_8C_3}\right)\cdot V_n \end{aligned} \tag{2}$$

The electronics circuit of the BSCS with individual components is presented in Fig. 3. In the design of the BSCS, three TL081 op-amps, two AD633 multipliers, three capacitors and six resistor elements having different values have been used. In order to demonstrate the circuit in a simple form, minor signals have been omitted on purpose. The operational amplifiers (op-amps) and multiplier units used in the circuit have been connected to a ±15 V power supply.

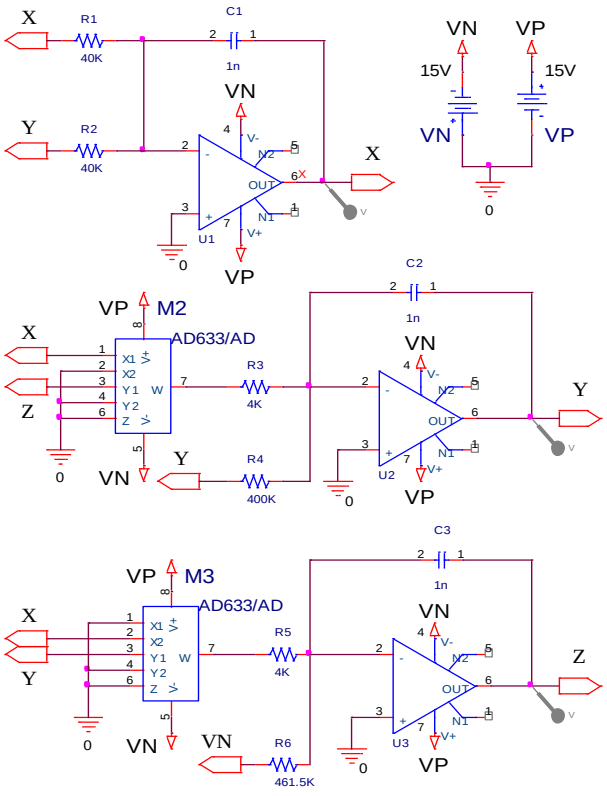

Fig. 3. Electronics circuit model of the BSCS.

The PSpice simulation results of the electronics circuit design of the system are presented in Fig. 4 (a), (b), and (c). Moreover, the system has been implemented with

individual analog circuit components. The oscilloscope outputs of the implemented system are presented in Fig. 5 (a), (b), and (c). As seen in Fig.5, the results obtained from the PSpice program verify the results of the physical circuit.

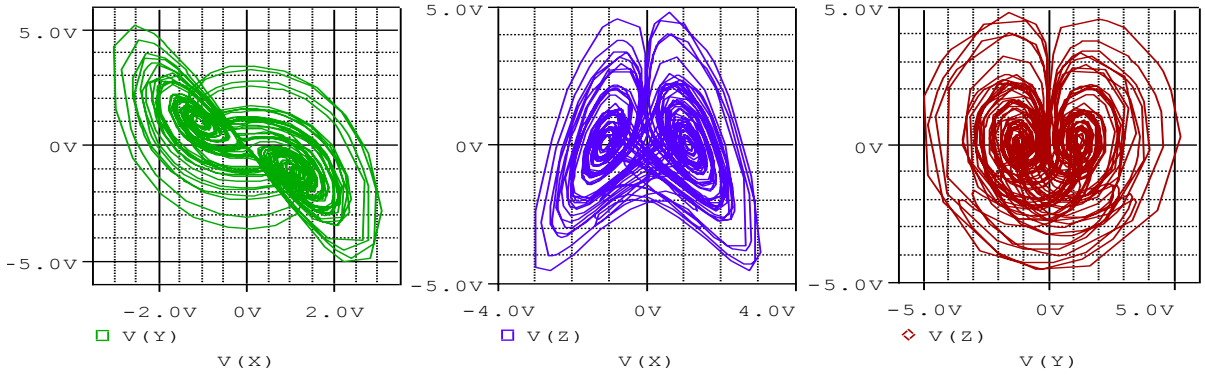

Fig. 4. PSpice simulation results of the Burke-Shaw chaotic oscillator
(a) x-y phase portrait (b) x-z phase portrait (c) y-z phase portrait.

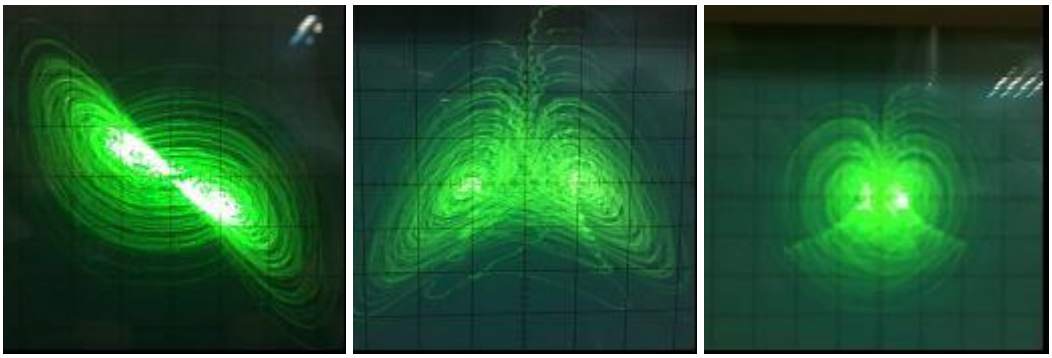

Fig. 5. Oscilloscope outputs of the realized Burke-Shaw chaotic oscillator.
(a) x-y signals phase portrait (b) x-z signals phase portrait (c) y-z signals phase portrait.

3. FPGA implementation of the BSCS and test results

In this study, the BSCS has been designed in hardware manner for the use of FPGA chips, in accordance with the 32-bit IEEE 754-1985 floating-point number standard. The designed chaotic unit has been coded in VHDL and synthesized with the Xilinx ISE 14.2 design platform for the Virtex-6 FPGA chip. Adders, dividers, multipliers, and other numerical primitive modules used during the design have been derived from Xilinx IP CORE Generator Tools. A block diagram of the chaotic unit designed with the RK5-Butcher algorithm can be seen in Fig. 6.

The 1-bit *Clock* and *Start* signals are used to ensure the synchronization between the chaotic oscillator and the system to which it is connected. The k_0, k_1, k_2, k_3, k_4, k_5, *and* ys units of the oscillator calculate the coefficients of the RK5-Butcher algorithm. The *ys* unit multiplies k_0, k_1, k_2, k_3, k_4, and k_5 values with fixed values in the algorithm and obtains the output signals of the oscillator and then transfers these values to a *filter* unit. The *filter* unit is used to filter error signals that can occur on the outlet of the chaotic oscillator. The 32-bit *X_S*, *Y_S*, and *Z_S* signals, which are output signals of the *filter* unit, are the signals generated by the chaotic oscillator. In addition, these signals are dispatched to the *MUX* as *x(k+1)*, *y(k+1)*, and *z(k+1)* signals, which will consequently be used to form initial conditions for the output signals to be generated by the oscillator at the moment of *t+1*. The duty of the *MUX* unit is to ensure the assigning of the initial conditions required by the system when the *Start* signal is asserted. In other words, this unit makes a choice between the initial conditions (*t0_x*, *t0_y*, and *t0_z*) assigned to the system by the user and the initial conditions obtained by the output of the system (*x(k+1)*, *y(k+1)*, and *z(k+1)*) and transfers these signals to the system. The 1-bit *R_XYZ* signal shows that the signals generated by the chaotic oscillator are ready. When the chaotic oscillator generates output signals, the *R_XYZ* signal is asserted as "*1*", and in other cases, it is "*0*".

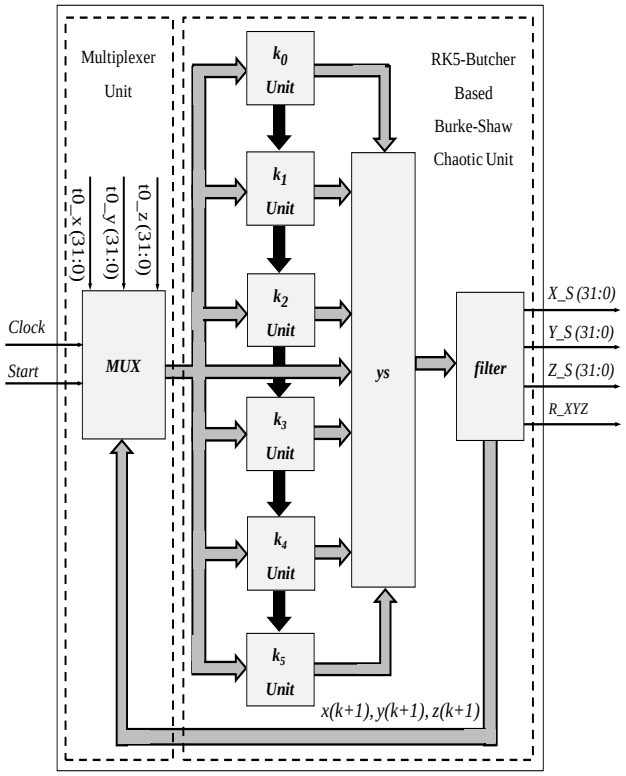

Fig. 6. Block diagram of Burke-Shaw chaotic oscillator unit.

The BSCS unit, which is implemented on an FPGA with RK-5 Butcher algorithm, is synthesized for XC6VCX75T chip, which is one of the smallest chips of Xilinx Virtex-6 family. Operating frequency of the designed unit is detected as 373.094 MHz by means of Xilinx ISE Design Tools 14.2 simulation program. The results of FPGA-based chaotic oscillator obtained from Xilinx ISE Simulator are presented in Fig. 7 that shows the values for the time series of *X_S*, *Y_S*, and *Z_S* outputs obtained from the implementation of the chaotic oscillator on an FPGA. The simulation results are demonstrated in a hexadecimal format in order to ensure easier analysis of the results.

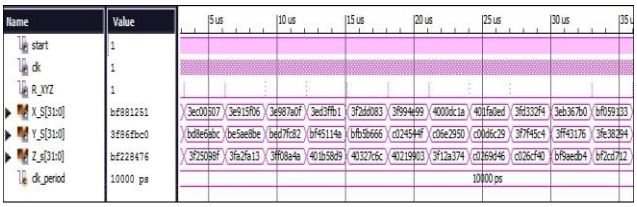

Fig. 7. Timing simulation results of FPGA-based Burke-Shaw oscillator.

The Virtx-6 XC6VLX550T FPGA chip statistics obtained from the Place-Route process which was conducted pursuant to the synthesizing process are presented in Table 1.

Table 1. FPGA chip statistics for the BSCS unit.

FPGA Chip	Number of Slice Regs. / %	Number of LUTs / %	Number of Occupied Slices / %	Number of Bonded IOBs / %	Max. Clock Frequency (MHz)
Virtex-6	80,190 / 11	79,967 / 23	24,203 / 28	99 / 11	373.094

4. Conclusions

In this study, the BSCS has been modeled numerically with the RK5-Butcher algorithm along with phase portraits and time series of the system are presented. Then, the chaotic system has been modeled with individual analog circuit components. Moreover, it is realized with discrete analog electronic circuit components. The results obtained from numerical modeling confirmed the validity of the modeling with the analog components. Finally, the Burke-Shaw chaotic system has been modeled on an FPGA by the use of the RK5-Butcher algorithm. The results of the FPGA-based and the numerical modeling are compared to each other and obtained results are better than earlier studies. According to the test results, the minimum operation period of the FPGA-based chaotic oscillator is 2.680ns. In addition, the FPGA-based chaotic oscillator unit is able to generate a 3.76 million-data set in one second.

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*Corresponding author: ismailkoyuncu@duzce.edu.tr