Calculation of the electrical parameters of aluminium/p type silicon diodes with and without the interfacial insulator layer using thermionic emission theory

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The effects of interfacial insulator layer on the electrical characteristics of Al/p-Si diodes have been investigated using the current–voltage (*I–V*) characteristics at room temperature. The values of ideality factor (*n*), barrier height (ϕ_b) and series resistance R_s have been determined from ln(*I*)-*V* plots, Cheung functions and the modified Norde functions. Electrical properties obtained from *I–V* characteristics of the device with interfacial insulator layer have been compared with the ones obtained from *I–V* characteristics of the device without interfacial insulator layer. The calculated ideality factor and barrier height are 1.49 and 0.595 eV for Al/p-Si diode, and 1.94 and 0.517 eV for Al/SiO_2/p-Si diode, respectively, and it is observed that the ideality factor (*n*) increases and barrier height (ϕ_b) decreases with interfacial insulator layer. The series resistance values obtained from Cheung functions of the diode with and without the interfacial insulator layer are R_s= 71 Ω and R_s= 112 Ω, respectively. Current–voltage characteristics and the power-law dependence was determined to be governed by space charge-limited currents (SCLC).

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1. Introduction

Due to the importance of the reliability and performance of Schottky diodes in the electronics industry, their electrical characteristics have been widely studied [1–7]. The fundamental parameters of the Schottky diodes are barrier height (ϕ_b) and ideality factor (*n*). Many studies have been carried out to control the barrier height and minimize the interface states at the interface of metal-semiconductor (MS) using some interfacial layers [1-7].

The effect of the presence of an interface insulator layer and interface states on the *I–V* characteristics of Schottky diodes have been studied by several authors [5-9]. The first studies on the interfacial layer in Schottky diodes were reported by Crowley and Sze [8] who obtained their estimations from an analysis of the barrier heights with different metallization as a function of metal work function. Hanselaer et al. [9] have measured the forward bias *I–V* characteristics of Schottky diodes with insulator layer and their results depicted a strong deviation from those of expected thermionic emission theory.

It is well known that an insulator layer can strongly influence the device characteristics such as the ideality factor, Schottky barrier height and the interface state density.

The performance and stability of these devices are especially dependent on the formation of an insulator layer and series resistance (R_s) [10]. For an accurate and reliable determination of the electrical characteristics, the Rs should be taken into account. The *I–V* measurements are one of the most popular electrical measurement techniques used to determine some important parameters of the Schottky diode. The aim of this study is to fabricate a Al/p-Si diodes with and without the interfacial insulator layer, examine the possibility of Schottky barrier diode formation using interfacial insulator layer and determine the electrical parameters such as the ideality factor, barrier height and series resistance of the diodes.

2. Experimetal details

The p-type Si wafer used in this study was (1 1 1) oriented, 350 μm thickness and 10 Ω-cm resistivity. Firstly, the wafer was chemically cleaned using the RCA cleaning procedure (i.e.10 min boil in $NH_3 + H_2O_2 + 6H_2O$ followed by a 10 min $HCl + H_2O_2 + 6H_2O$). Preceding each cleaning step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ-cm. Secondly, the ohmic contact was made by evaporating 1500 Å thick Al in

a vacuum of 1×10^{-6} Torr on the back of the substrate and annealed at 500 ^{o}C for 2 min in N_2 atmosphere. In order to remove the native oxide on surface on p-Si, the substrate was etched by HF:H_2O (1:10) and then was rinsed in deionized water using an ultrasonic bath for 10 min. the wafer was cut into two pieces: one was immediately inserted into the evaporation chamber for forming the Al/p-Si (MS) Schottky diodes, and the other piece was exposed to clean room air for 30 days at room temperature before Schottky contact evaporation in order to obtain a native insulator layer on the clean p-Si MIS ((metal–insulator layer–semiconductor) Schottky diode). Finally, to form the Schottky contacts, the circular dots of 2 mm diameter and 1500 Å thick Al are deposited onto the with and without oxidized surface of the wafer in vacuum system in a vacuum of 1×10^{-6} Torr. The *I–V* measurements of the device were performed by Keithley 2400 electrometer at room temperature.

3. Theoretical procedures

3.1. Thermionic emission theory

The thermionic emission theory can be used to obtain electrical properties of the Schottky diodes. According to the theory, the net current of a Schottky diode with a series resistance is given by [1]:

$$I = I_0 \exp\left(\frac{q(V - IR_s}{nkT}\right) \tag{1}$$

where I_0 is the saturation current and written as [1]

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \tag{2}$$

The ideality factor (n) and the barrier height (ϕ_b) of the diodes can be calculated using Eqs. (1) and (2) from the slope and the *y*-axis intercept of the linear region of ln*I*-*V*, respectively.

$$n = \frac{q}{kT}\frac{dV}{d(\ln I)} \tag{3}$$

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \tag{4}$$

where ϕ_b is the zero bias barrier height, n is the dimensionless ideality factor, q is the electron charge, A* is the Richardson constant and equals to 32 Acm^{-2} K^{-2} for p-Si [1], A is the effective diode area, T is the absolute temperature, k is the Boltzman constant, R_s is the series resistance and V is the applied voltage.

3.2. Cheung theory

The values of the series resistance (R_s) of the MS and MIS Schottky diodes were obtained from the forward bias *I–V* data using the methods developed by Cheung and Cheung [11]. The forward bias current–voltage characteristics due to the thermionic emission of Schottky diodes with the series resistance can be expressed as [11] Cheung's functions:

$$\frac{dV}{d\ln(I)} = IR_s + n\frac{kT}{q} \tag{5}$$

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\phi_b \tag{6}$$

3.3. Modified Norde theory

The electrical parameters of the MS and MIS diodes can also be evaluated from modified Norde method [12]:

$$F(V) = \frac{V}{a} - \frac{kT}{q}\left(\frac{I(V)}{AA^*T^2}\right) \tag{7}$$

where a is a the first integer greater than n and $I(V)$ is the current obtained from the *I–V* curve.

The barrier height of the MS and MIS diodes can be calculated by using [12]:

$$\phi_b = F(V_0) + \frac{V_0}{a} - \frac{kT}{q} \tag{8}$$

where $F(V_0)$ is the minimum $F(V)$ value of F vs. V graph and V_0 is the corresponding voltage. The series resistance (R_s) can be obtained by the Norde's method through the relation [12]:

$$R_s = \frac{kT(a-n)}{qI} \tag{9}$$

4. Result and discussion

Fig. 1 shows the room temperature experimental forward and reverse bias *I–V* characteristics of Al/p-Si Schottky diodes with and without a interfacial insulator layer. The experimental values of ideality factor (n) and barrier height (ϕ_b) were calculated as 1.49 and 0.595 eV for the Al/p-Si (MS) Schottky diode and 1.94 and 0.517 eV for Al/SiO_2/p-Si (MIS) Schottky diode using Equations (3) and (4), respectively.

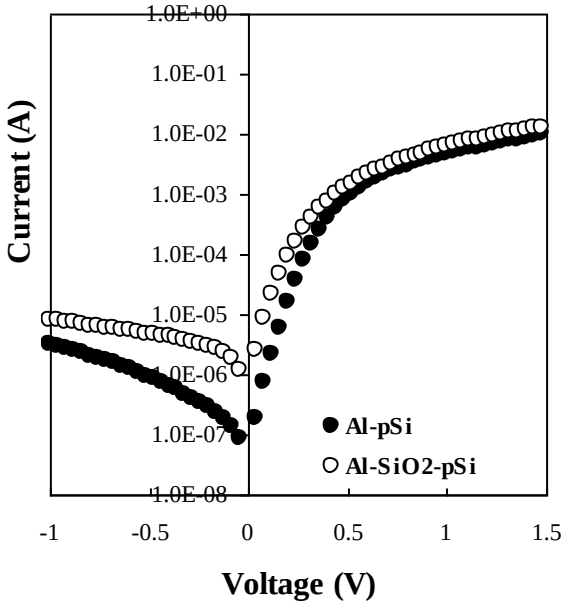

Fig. 1. The plots of the current–voltage (I–V) characteristics for Al/p-Si and Al/SiO_2/p-Si Schottky diodes.

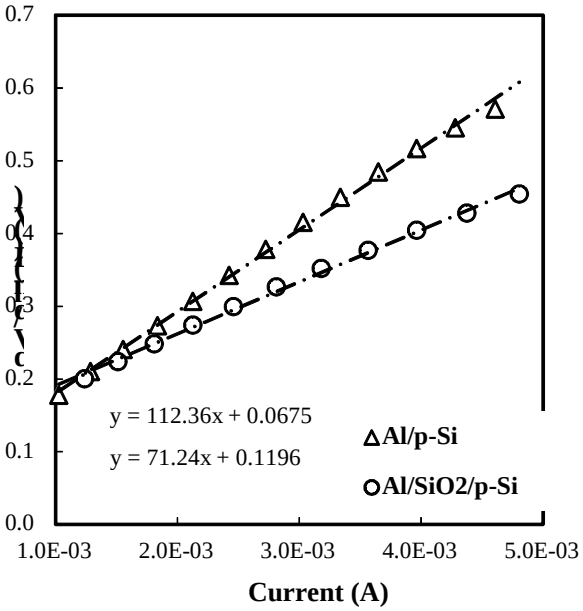

Fig. 2. The experimental dV/d(lnI)-I plot for the Al/p-Si and Al/SiO_2/p-Si Schottky diodes.

The high values of ideality factor can be attributed to the effects of the bias voltage drop across the insulator layer (SiO_2) between metal and semiconductor and series resistance [5-7]. This suggests that the effect of series resistance on the diode parameters cannot be ignored [1,2]. When the electrical properties of Al/p-Si diode are compared with Al/SiO_2/p-Si diode, the barrier height (ϕ_b = 0.515 eV) of Al/SiO_2/p-Si diode at the room temperature is lower than that of the Al/p-Si Schottky diode (ϕ_b = 0.595 eV) and the ideality factor (n = 1.94) of Al/SiO_2/p-Si diode is higher than that of the Al/p-Si Schottky diode (n = 1.49) at the room temperature.

Several methods to extract the series resistance R_s of a device have been suggested [11,12]. In order to calculate series resistance in the device with high ideality factor and series resistance, Cheung's method [11] can be used. Figs. 2 and 3 show the plots of dV/d(ln$I$)–I and $H(I)$–I for the diodes. The n, R_s and ϕ_b values were determined using Eqs. (5) and (6) from the plots of dV/d(ln I) –I and $H(I)$–I. The values of n and R_s were calculated as 2.61 and 112 Ω for Al/p-Si (MS) Schottky diode and 4.62 and 71 Ω for Al/SiO_2/p-Si (MIS) Schottky diode from the intercept and the slope of Fig. 2, respectively. The values of ϕ_b and R_s were calculated as 0.741 eV and 117 Ω for Al/p-Si (MS) Schottky diode and 0.660 eV and 92 Ω for Al/SiO_2/p-Si (MIS) Schottky diode from the intercept and the slope of Fig. 3, respectively. The results show the consistency of the method. In addition to Cheung's method, the modified Norde method [12] can be used to calculate the ϕ_b and R_s parameters of the diodes.

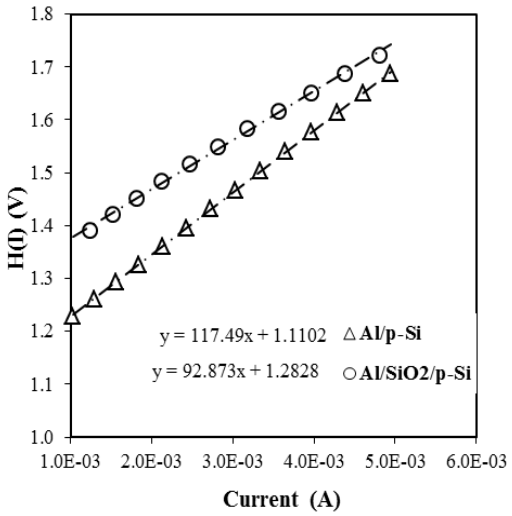

Fig. 3. The experimental H(I)-I plot for the Al/p-Si and Al/SiO_2/p-Si Schottky diodes.

Fig. 4 shows the $F(V)$–V graphs of the Al/p-Si (MS) and Al/SiO_2/p-Si (MIS) Schottky diodes. The barrier height (ϕ_b) and the series resistance (R_s) values were calculated using Eqs. (8) and (9) as 0.711 eV and 43 Ω for Al/p-Si (MS) Schottky diode and 0.687 eV and 30 Ω for Al/SiO_2/p-Si (MIS) Schottky diode, respectively. The series resistance and the barrier height values obtained from both methods (Norde and Cheung) are different from each others.

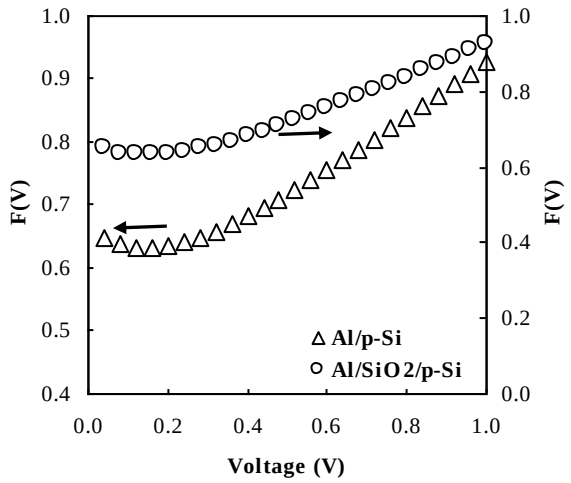

Fig. 4. F(V) - V graph of the Al/p-Si and Al/SiO2/p-Si Schottky diodes.

The barrier height (ϕ_b) and series resistance (R_s) values determined from Norde's method is lower than the one obtained from Cheung's method.

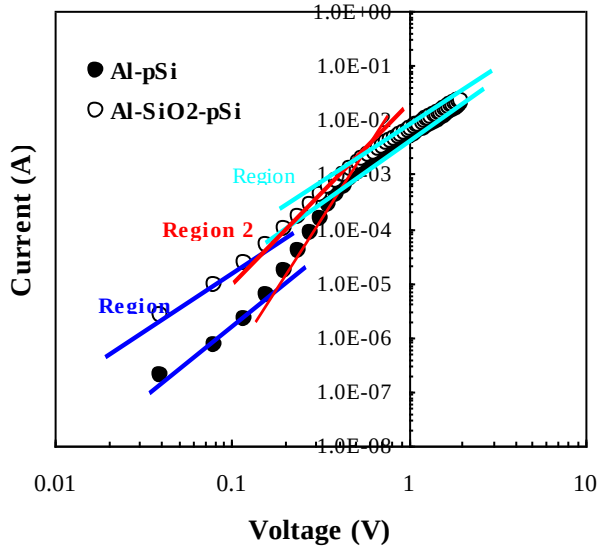

Fig. 5. The forward bias log(I)-log (V) plot of the Al/p-Si and Al/SiO$_2$/p-Si Schottky diodes.

Fig. 5 shows the forward bias ln(I) versus ln(V) plots of the Al/p-Si and Al/SiO$_2$/p-Si Schottky diodes at room temperature. As can be seen from this figure, the forward bias characteristics show three distinct regions change in the form of $I \propto V^m$ at each diode. The curves of Fig. 5 show voltage dependence, followed by power law dependence at higher voltage region. This behaviour can be attributed to space charge limited current (SCLC). The region I shows low bias with 2.18 and 1.92 m value for the Al/p-Si and Al/SiO$_2$/p-Si Schottky diodes, respectively. The region II shows low bias with 4.58 and 3.03 m value for the Al/p-Si and Al/SiO$_2$/p-Si (MIS) Schottky diodes, respectively. The region III shows low bias with 2.43 and 2.26 m value for the Al/p-Si and Al/SiO$_2$/p-Si Schottky diodes, respectively. The m values determined for the Al/SiO$_2$/p-Si diode is lower than the one obtained for the Al/p-Si diode for three regions.

5. Conclusion

The current–voltage (I-V) characteristics of Al/p-Si diode with and without interfacial layer have been investigated. Using thermionic emission theory, Cheung theory and modified Norde theory, the characteristics diode parameters such as the ideality factor, barrier height and series resistance were extracted from the I-V electrical measurements of the each diode.

Although the ideality factor values obtained for Al/SiO$_2$/p-Si Schottky diode is higher than the ones obtained for the Al/p-Si Schottky diode, the barrier height values obtained for Al/SiO$_2$/p-Si Schottky diode is lower than the ones obtained for the Al/p-Si Schottky diode.

The space charge limited conduction (SCLC) mechanism in Al/p-Si Schottky diode with and without interfacial oxide layer was also investigated. The ln(I)–ln(V) curves of the diodes exhibit three regions change in the form of $I \propto V^m$. The curves show voltage dependence, followed by power law dependence at higher voltage region. This behaviour can be attributed to space charge limited current (SCLC).

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