Characteristics of silicon oxide film for low voltage-driven CE chip

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Silicon oxide film was deposited on glass substrates by electron-beam evaporation. Different conditions for the preparation of the SiO_2 film were studied. Micro-morphology, thickness and compositions of SiO_2 film were investigated by AFM, surface profiler and XRD. Metal-insulator-metal structures have been used to measure the electrical properties of the film. Experiment result shows that the surface of SiO_2 film became smooth and uniform for the growth temperature at 300℃, the breakdown voltage was higher than 200V for the thickness of the film at 4μm. This SiO_2 film meets the requirements as the insulation film for the low voltage-driven Capillary electrophoresis chip.

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1. Introduction

Capillary electrophoresis chip (CE chip) as a kind of microfluidic device has proven to be a powerful platform to achieve the separation and detection of bio-sample on a microchip. The device has clearly demonstrated the advantages of miniaturization, high efficiency and low sample consumption. It also presents a promising application in the analysis of peptide, hormone and drug screening [1-5]. However the injection and separation of samples in the conventional CE chips require high voltage from several hundreds to thousand volts, the large power equipment is difficult to integrate. Therefore, a kind of arrayed-electrode CE chips with low circulation voltage need to be developed.

Lin introduced the concept and principle of low voltage-driven CE chip, where moving electrical fields was used for the reagent separation [6].Wu analyzed the separation indexes and simulated the electrical field model of CE chip [7]. But in the application of the chip, sample solution in the micro-channel should contact with the microelectrodes directly. While the voltage is applied on the CE chip, the water in the channel could be electrolyzed and the bubbles are generated near the electrodes. Subsequently, the bubbles block the micro-channel and interrupt the sample separation process. This hinders the development of the low voltage-driven CE chip, some researchers have investigated this problem and proposed several methods [8-10], but the outcomes were not promising.

To solve the issue, a low voltage driven CE chip with a SiO_2 insulation film fabricated by electron-beam evaporation was presented by our group. The deposited SiO_2 film on the arrayed electrodes avoids contact between the electrodes and sample, so the sample solution flow through the channel smoothly and its separation could be accomplished.

2. Experiment

The SiO_2 films were deposited by the electron beam evaporation system (ULVAC HPS-510S). The main vacuum chamber of the system was pumped down to the pressure 2×10^{-3} Pa and the SiO_2 target were evaporated at 4×10^{-3} Pa. Substrate temperature was varied from room temperature to 300℃ with an accuracy of ±1℃and the film growth rate ranged from 0.1nm/s to 2nm/s, depending on the filament current of the electron beam. Thickness of the film was measured using a surface profiler ET4000 (Kosaka Laboratory Ltd). The crystal structure and the phase formation of the thin films were analyzed by Rigaku D/max-2400 (Cu Kα radiation 40kv, λ=1.54060Å) diffractometer. The surface morphologies were carried out with atomic force microscope (model: Digital Instruments Nano-Scope III). *C-V* and *I-V* characterization was performed by an Agilent B1500A semiconductor device analyzer and a Keithley 2612 source measurement unit with a probe station equipped at room temperature.

3. Results and discussion

3.1. Morphology

The surface morphology of the deposited SiO_2 film is observed using AFM. Fig. 1(a) shows the surface morphology of the 150 nm film deposited on the substrate at room temperature. It can be seen that the

grain-like features is visible, the SiO_2 particles are big and distribute homogeneously, whereas some pinholes exist. The surface mean roughness (Ra) value is 0.81 nm. The substrate temperature is reached to 300℃ and the thickness of the film remains 150 nm, the surface morphology of the film is shown in Fig. 1(b). We can see that the SiO_2 particles are distributed uniform and arranged closely, pinholes rarely appeared, but there are still some big particles (the bright part). The surface of the film Ra value was 0.66 nm. The film increased from 150 nm to 4 μm under substrate temperature of 300℃ is shown in Fig. 1(c), it is found that the surface is more compact and uniform, and the film Ra is reduced to 0.27nm. The results can be explained that the SiO_2 particles are deposited on the substrate, which is a nucleation and growth process, the particles move slowly and the grain size is big at low temperature which results in rough surface and has many pinholes.

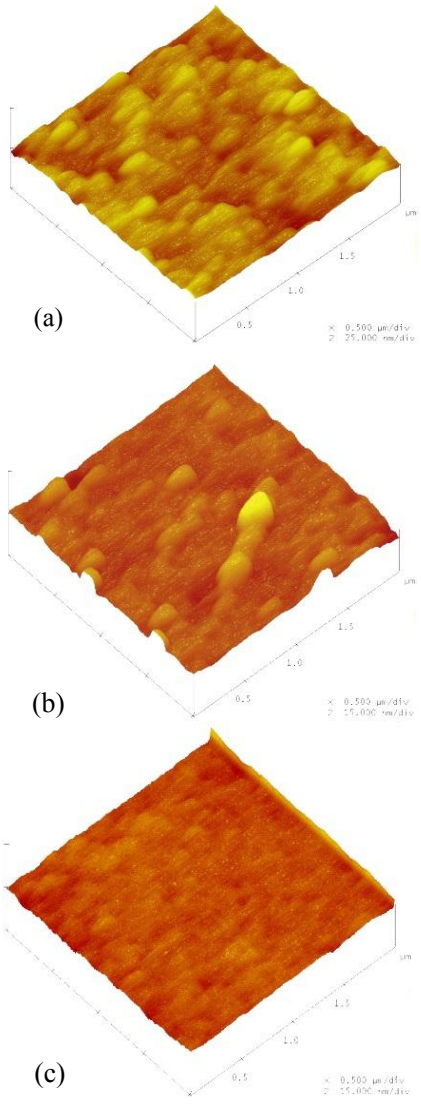

Fig. 1. AFM images of the surface of SiO_2 film on different conditions (a) 150nm thick film is deposited at room temperature (b) 150 nm thick film is deposited at 300 °C (c) 4μm thick film is deposited at 300 °C.

The substrate temperature increases, the particles could not cool down immediately, so that the diffusion effect is enhanced and the surface become smoother. As the thickness of the film is small, a few parts show the island like structure. However, the compactness of the film increases with the film thickness increasing at the high substrate temperature, the SiO_2 particles continue to fill the pores and cracks generated before, a dense and smooth film structure is formed.

3.2. Structural characterization

The X-ray diffractometry (XRD) studies are performed on the film to examine the phase formation and crystal structure [11-12]. Fig. 2 shows the XRD pattern of the SiO_2 film at the substrate temperature of 300℃. It is found that the film was amorphous in nature since there were no significant peaks found except one broad peak which is the characteristic peak of the glass. Generally, as the film is crystal structure, impurity atom may move and accumulate along the grain boundaries and steam would permeate the boundaries, the electric breakdown is easy to occur, but the amorphous film is desirable to reduce this effect, which breakdown filed is higher than crystal structure [13].

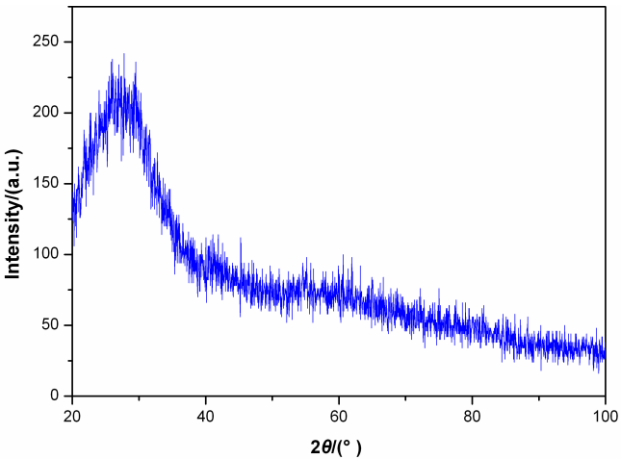

Fig. 2. XRD pattern for the SiO_2 film.

3.3 Electrical properties

To study the electrical properties of the SiO_2 films, a MIM (Al/SiO_2/Al) structure was fabricated in Fig. 3 [14-15]. A metallic aluminum layer was prepared on the glass by RF magnetron sputtering as the bottom electrode. The top electrodes (Al, circular dots, Φ=200μm) were deposited by thermally evaporating on the surface of the SiO_2 films [16-18]. During the electrical properties measurement, the top electrode was biased while the bottom electrode was grounded.

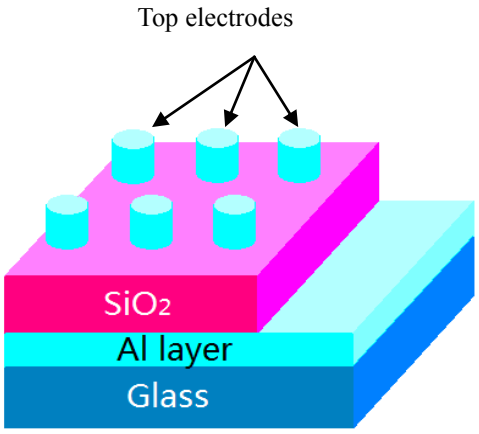

Fig. 3. The MIM structure for SiO_2 thin film characterization.

Fig. 4 shows a plot of *C-V* characteristics taken in the frequency 1MHz and the inset gives capacitance density versus applied frequency for the SiO_2 film of thickness 150nm deposited at 300 °C. It shows that there are some fluctuations of the capacitance density ranging form 0.155 fF/μm^2 to 0.137 fF/μm^2 with the voltage; the capacitance decrease with the function of frequency. This indicates that the film is less dense and the charge traps have an effect at lower frequencies [19].

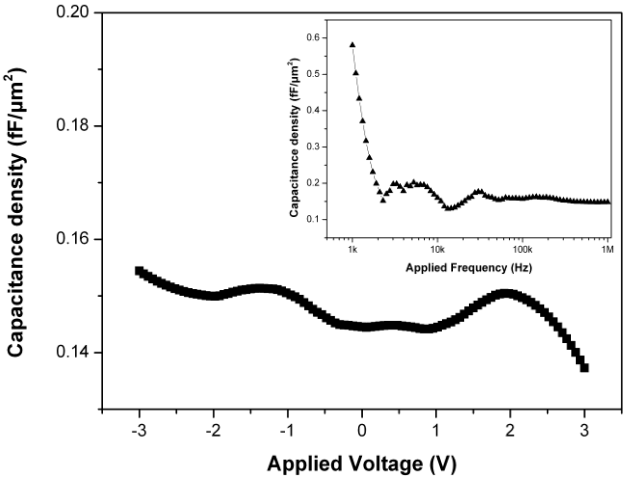

Fig. 4. C-V and Capacitance density VS. applied frequency for SiO_2 film of thickness is 150 nm.

Fig. 5 presents the *C-V* for the 4μm SiO_2 film deposited at 300℃ in 1MHz and the inset shows the plot of capacitance density versus applied frequency. It was observed the capacitance density of the thick SiO_2 film is stable with respect to the voltage and frequency which is around 0.00709fF/μm^2. The increase in grain size favors the reduction of the bulk trap density, so there are a much smaller number of charge traps near the electrode interfaces which became inactive with the increased frequency. The 4μm SiO_2 film improves the performance of the MIM capacitor in terms of stability with the frequency and it is a lesser porosity, lesser defects and higher uniform insulation film [20].

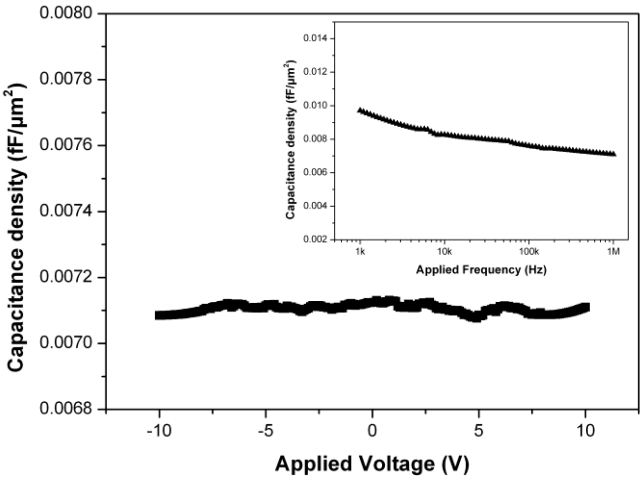

Fig. 5. C-V and the inset gives Capacitance density VS. applied frequency for SiO_2 film of thickness is 4μm.

Fig. 6 shows the current–voltage curve of the SiO_2 film at different thickness deposited at 300 °C. In Fig. 6 (a) the evaporated SiO_2 film is 150 nm, the leakage current density increase with the applied electrical field strength, but there are some slight decreases in growth. It is a typically the NDR (negative differential resistance) characteristics in the MIM structure. As the electric field was up to 235 KV/cm, the current density was increased rapidly from 10^{-5}A/cm^2 to more than 0.5 A/cm^2, the film breakdown occurred. Fig. 6 (b) shows the plot of *I/V* for the SiO_2 film with 4μm thickness, a similar trend had been observed, the value of breakdown electric field which was more than 500 KV/cm with the breakdown voltage above 200V.

It can be seen from the Fig. 6, the current density of the 4 μm SiO_2 film was obviously higher compared with 150 nm thick SiO_2 film. This is related to the grain boundaries that is the interface of one grain contacts with another. At the grain boundaries, there are various kinds of defects which influence the bulk trap density. The capability of capturing free carriers depends on the formation of trapping states. With the increasing of the film thickness the effective grain boundaries decreases, the ionization energy of the defects and the scattering effect reduces. So the carrier concentration and carrier mobility of the SiO_2 film was enhanced which leads to increase the leakage current [21]. Because the compactness and the thickness boost up, the breakdown voltage of the film became higher at the same, it satisfies the demand of the voltage driving for the capillary electrophoresis chip.

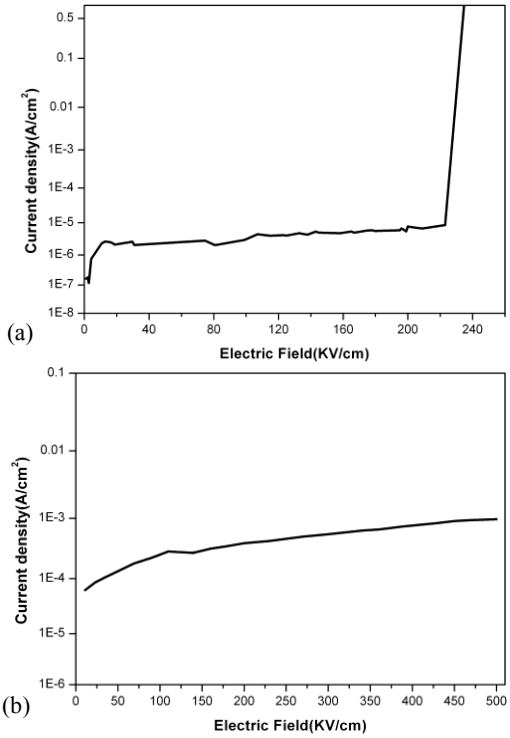

Fig. 6. I/V characteristics of SiO_2 thin film (a) film thickness is 150nm (b) film thickness is 4μm.

3.4 Chip Design

In order to reduce the injecting and separating voltage, the arrayed electrodes were designed both in the injecting and separating channels. All the arrayed electrodes were fabricated on a piece of glass substrate, and the crisscross micro channel and the reservoirs were processed on the other glass cover. The width of each of the electrodes is 100 μm and the distance between the parallel electrodes is about 600 μm, the area of the welding plate is 250 μm × 250 μm. The arrayed electrodes of titanium and the platinum were fabricated on the glass substrate by RF sputtering. The thickness of the electrode is about 200 nm. The crisscross micro channel of capillary electrophoresis was fabricated with wet etching method and four holes were drilled by ultrasonic. Since the substrate and cover plate of chip are both glass, the material properties of the deposited SiO_2 insulation film are similar with it, the high temperature sealing technology was used for the chip boding. The Fig. 7 shows the capillary electrophoresis chip deposited the 4μm SiO_2 insulating film with arrayed electrodes bonded successfully; welding plates of the chip were connected to the PCB pad by the gold filament [22].

Fig. 7. Successful bonding chip attached the PCB board.

3.5 Chip experiment

To verify the ability of the SiO_2 insulation film for isolating sample electrolyze, the buffer was driven through the micro channel of bonded low voltage-driven CE chip by the low voltage driven system. In the separation process, the maximum driven voltage applied on the arrayed electrode pairs was about 150V. Fig. 8 shows the buffer solution in the chip with different insulation films was driven by applied voltage. The perpendicular black straight lines were electrodes; the horizontal one was separating channel which filled with the sample solution. The insulation efficiency for the chip using silicon nitride film is shown in Fig. 8(a), it was found that some bubbles were generated near the electrodes, the bubbles were getting larger and larger with time, finally resulting in completely blocking the micro channels and interrupting the separating process. The reason can be explained that the silicon nitride film has some micro fissures, so the buffer contact with the electrodes through the film, the solution was electrolyzed. The insulation effect using 4μm SiO_2 film for the chip is shown in Fig. 8 (b), it can be seen that bubble was not produced in the near the electrodes. This demonstrates that the films is compact and withstand high voltage, which could accomplish the sample separation.

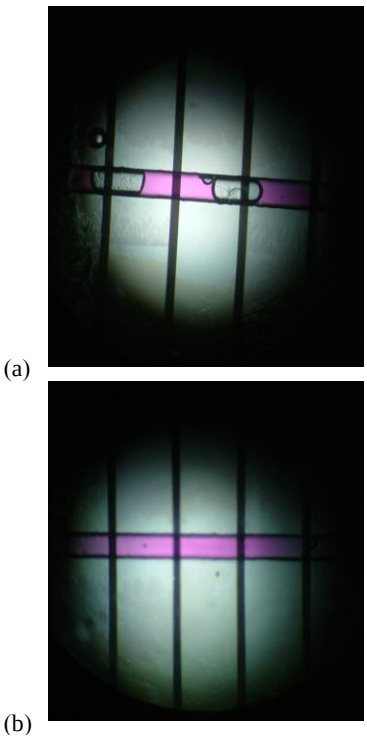

Fig. 8. Sample driven by the low voltage system using different insulation film (a) using silicon nitride film (b) using SiO_2 film.

4. Conclusions

E-beam evaporated SiO_2 as the insulation film was prepared for the low-voltage driven CE chip to avoid

directly contacting between electrode and liquid sample. With the instruments of XRD and AFM, the SiO_2 film grown at 300 ^oC with the thickness of 4 μm was amorphous and uniform with less pinholes and defect. The insulating characteristics of the 4 μm SiO_2 film is studied that the breakdown voltage is higher than 200V. The sample test shows that there is no obviously bubble in the micro channel. These experimental results suggest that the SiO_2 is a promising insulation film for the low-voltage driven CE chip and other electronic application.

Acknowledgements

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Reference

[1] A. Manz, D. J. Harrison, E. M. J. Verpoorte, J. C. Fettinger, A. Paulus, H. Lüdi, H. M. Widmer, Journal of Chromatography A **593**, 253 (1992).
[2] A. Brown, C. Morales, F. A. Gomez, Talanta **74**, 605 (2008).
[3] Z. Xu, Y. Lan, X. Fan, Q. Li, Talanta **78**, 448 (2009).
[4] C. Rivet, H. Lee, A. Hirsch, S. Hamilton, H. Lu Chem Eng Sci **66**, 1490 (2011).
[5] H. F. Lv, W. P. Yan, L. Pan, Sensor Letters **9**, 755 (2011).
[6] Y. C. Lin, Sensors and Actuators B: Chemical **80**, 33 (2001).
[7] Y. Wu, Z. Y. Wen, Z. Y. Zhang, Optics and Precision Engineering **11**, 130 (2003).
[8] K. A. D. Guzman, R. N. Karnik, J. S. Newman, A. Majumdar, Microelectromechanical Systems, Journal of **15**, 237 (2006).
[9] Y. Z. Wang, Z. Zhao, Instrument Technique and Sensor **3**, 237 (2006).
[10] H. N. Li, W. P. Yan, J. M. Liu, Chinese Journal of Scientific Instrument **27**, 2488 (2006).
[11] L. Zhang, H. C. Jiang, C. Liu, J. W. Dong, P. Chow, Journal of Physics D: Applied Physics **40**, 3707 (2007).
[12] R. K. Gupta, K. Ghosh, R. Patel, P. K. Kahol, Journal of Physics D: Applied Physics **45**, 085002 (2012).
[13] W. X. Weng, Z. Jia, G. L. Yu, Journal of Fuzhou University **39**, 67 (2011).
[14] T. Peter, S. Beate, D. Detlef, H. Eckart, New Journal of Physics **12,** 113014 (2010).
[15] D. Prime, S. Paul, P. Josephs-Franks, Dielectrics and Electrical Insulation, IEEE Transactions on **15**, 905 (2008).
[16] Ahmetoglu Muhitdin, Tekgul Atakan, Alper Mursel, Optoelectron. Adv. Mater.-Rapid Commun. **6**, 292 (2012).
[17] C. Bondoux, P. Prené, P. Belleville, F. Guillet, S. Lambert, B. Minot, R. Jérisian, Journal of the European Ceramic Society **25**, 2795 (2005).
[18] E. D. Popescu, T. Gavrila Zaharescu, Optoelectron. Adv. Mater.-Rapid Commun **5**, 1056 (2011).
[19] E. Hourdakis, A. G. Nassiopoulou, Microelectronic Engineering **90**, 12 (2012).
[20] J. P. Kar, G. Bose, S. Tuli, Current Applied Physics **6**(5), 873 (2006).
[21] J. S. Zhang, Y. E. Q., F. Q. Zeng, Materials Review **25**, 301 (2011).
[22] N. Xue, W. P. Yan, Sensors and Actuators A: Physical **173**, 145 (2012).

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