Design and FPGA implementation of reconfigurable OFDM with improved PAPR

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The Orthogonal Frequency Division Multiplexing (OFDM) is used in various modern day wireless standards. It can be realized in two ways namely, Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT). The OFDM-FFT shows a performance improvement in terms of area, speed and power but fails to improve Peak-to-Average-Power-Ratio (PAPR). On the other hand the OFDM-DWT shows a promising improvement in terms of PAPR. This paper presents a reconfigurable Orthogonal Frequency Division Multiplexing (OFDM), which will configure between the Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT) based on the application needs. The proposed reconfigurable OFDM is developed using Verilog HDL and targeted in Xilinx Virtex 5 FPGA (xc5v1x30ff324). The proposed OFDM shows a remarkable performance improvement in terms of Peak-to-Average-Power-Ratio (PAPR) at the cost of area overhead. The area overhead is due to the Discrete Wavelet Transform (DWT) architecture which consumes 16.14% more Gate Element (GE) than the Fast Fourier Transform (FFT) architecture. However, the proposed architecture with shared resources saves 58.67% and 57.05% sliced LUT and Gate Element (GE) respectively.

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1. Introduction

The vital component in mobile and wireless communication is Orthogonal Frequency Division Multiplexing (OFDM) [1]. The Orthogonal Frequency Division Multiplexing technique is used in various wireless standards such as Wireless Local Area Network (WLAN) [2], WiMAX [3], and Digital Video Broadcasting – Terrestrial [4]. The Orthogonal Frequency Division Multiplexing (OFDM) [5] consists of the Mapper, Serial-to-Parallel converter, Pilot insertion block, Inverse Fast Fourier Transform (IFFT), Parallel-to-Serial converter, Analog-to-Digital (ADC) unit, Fast Fourier Transform (FFT) and Digital-to-Analog (DAC) unit. OFDM follows multi-carrier technique, where the many carriers are obtained by splitting the spectrum. The digital modulation of the original message is carried out as the initial process of OFDM. Then the Fast Fourier Transform (FFT) will convert the time domain signal to frequency domain signal.

The Inverse Fast Fourier Transform (IFFT) will reverse the operation of FFT. The increasing need of mobile applications in the fast growing technology, require this Orthogonal Frequency Division Multiplexing (OFDM) as Intellectual Property (IP) to integrate with the applications. As the technology size shrinks, the Orthogonal Frequency division Multiplexing (OFDM) should maintain its efficiency in terms of area, speed (i.e. data rate), power, Bit Error Rate (BER) and Peak to Average Power Ratio (PAPR). On the other hand, the Orthogonal Frequency Division Multiplexing (OFDM) can be developed using Fast Fourier Transform (FFT)/Inverse Fast Fourier Transform (IFFT) and Discrete Wavelet Transform (DWT)/Inverse Discrete Wavelet Transform (IDWT). The OFDM based on IFFT/FFT has several advantages such as, low computation time of FFT/IFFT algorithms, area and power. But it fails to achieve low Peak to Average Power Ratio (PAPR) and there is a synchronization problem. In contrast to this, the OFDM based on Discrete Wavelet Transform (DWT)/Inverse Discrete Wavelet Transform (IDWT) shows a promising result in terms of PAPR. The idea of the paper evolved here to combine both IFFT/FFT and IDWT/DWT in a single OFDM. The idea is developed by utilizing the art of Reconfigurability [6]. The reconfigurable architecture will utilize the same area based on the reconfigurable logic developer. This paper presents the reconfigurable Orthogonal Frequency Division Multiplexing (OFDM), which will change between Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT).

2. Related works

The OFDM [7] based on dynamic partial reconfigurable between FFT/IFFT is used to achieve area and power efficiency. The architecture for variable length FFT/IFFT for OFDM is proposed in [8], where FFT/IFFT point can be varied. The pipelined FFT [9] is used to reduce the complexity in MIMO OFDM. The coded

MIMO OFDM is analyzed in terms of Bit Error Rate (BER) in [10]. The data rate of OFDM is improved using beam forming technique and space-time coding [11]. The architecture [12] for resource allocation in OFDM based on varying channel condition is proposed to maintain the throughput of the OFDM at low Bit Error Rate (BER). The multiplier-less FFT [13] for OFDM is implemented to improve the performance of OFDM, in terms of area. The Peak to Average Power Ratio (PAPR) in OFDM is reduced by Boolean Particle Swarm intelligence Optimization (BPSO) [14], the inter-weight and phase-weight has added to the reduction parameters. In [15], a new technique of PSO-ACE-POCS is proposed to reduce the Peak to Average Power Ratio (PAPR). The PAPR performance of the OFDM is reduced by a hybrid method [16], which combines the Conventional Partial Transmit Sequence (C-PTS) with clipping and interleaving methods. A novel technique [17] of unused tones along with the phase information is used to reduce the Peak to Average Power Ratio (PAPR) in Orthogonal Frequency Division Multiplexing (OFDM).

The area efficient and low power Fast Fourier Transform (FFT) [18] is proposed for Orthogonal Frequency Division Multiplexing (OFDM). The OFDM with high data rate is achieved by implementing the modified Fast Fourier Transform (FFT) processor [19]. Many works have been contributed to the development of Orthogonal Frequency Division Multiplexing (OFDM) based on Fast Fourier Transform (FFT) but the Peak to Average Power Ratio (PAPR) is a major concern with this type of realization. Hence, the OFDM based on Wavelet transformation is considered as the alternate solution. The comparison of OFDM [20] based on Discrete Wavelet Transform (DWT) and Fast Fourier Transform (FFT) shows the promising improvement in Bit Error Rate (BER). The orthogonality of the OFDM is improved by the feature extraction based on eigenvector/eigenvalues [21], also the novel approach show remarkable performance in terms of PAPR and BER. The survey of Wavelet families [22], that suits the OFDM under various noisy channels is analysed for BER improvement over the conventional OFDM. In [23], the frequency resolution of the sub-carrier signal is improved by utilizing the property of Wavelet Packet Transform (WPT) and the results are compared with conventional OFDM based on FFT and DWT. The computational complexity of IFFT in OFDM is reduced by wavelet transform and the proposed OFDM [24] shows high flexibility when implemented in DVB-T. In [25], the reconfigurable architecture for different wireless standard is proposed. The architecture will reconfigure between the WCDMA and OFDM standard. The idea of our paper is evolving here to propose, hardware architecture for OFDM that will reconfigure between Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT). In [25], the reconfigurable receiver architecture with WCDMA and OFDM is implemented by Rake Finger and FFT respectively. To simplify our proposed work, the FFT implementation of OFDM [25] is used in our work along with the proposed reconfigurable architecture of wavelet transform for OFDM.

3. Proposed reconfigurable OFDM

The proposed reconfigurable Orthogonal Frequency Division Multiplexing (OFDM) is shown in Fig. 1. This OFDM architecture will able to reconfigure between different Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT). The proposed design employs the reconfigurable functional block [26] and reusable functional block [27]. This reusable and reconfigurable architecture, functional blocks is used to implement FFT and DWT algorithm used in OFDM.

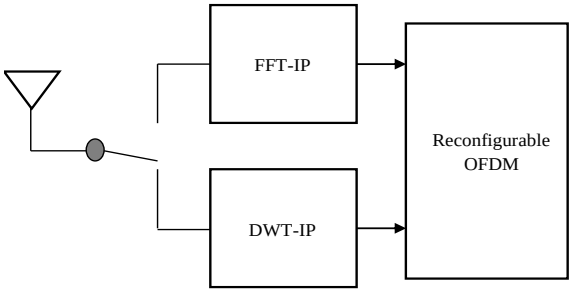

Fig. 1. Proposed Reconfigurable OFDM.

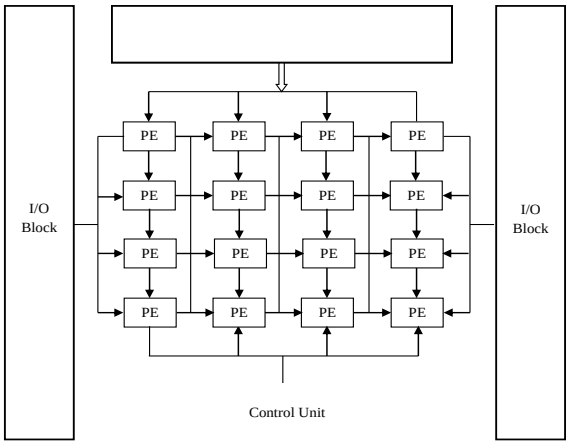

Fig. 2. Components in Proposed Reconfigurable Architecture.

The process of the MAC unit along with addition and subtraction are implemented using few reusable functional blocks. These processes are in turn used to implement the reconfiguration between FFT and DWT. The various components included in the proposed OFDM architecture are shown in Fig. 2 such as I/O blocks to send and receive data from various blocks, memory block to store the instruction, data and buffer data, control block and Processing Elements (PE). The proposed OFDM architecture will able to switch from Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT) core based on demand with the help of various blocks and

meanwhile the switching is based on the application requirement.

4. Implementation Fast Fourier Transform (FFT)

As mentioned earlier, the FFT implementation [25] is exposed here, and in this paper the Real and Complex number is denoted by 'R' and 'C'. The 64-point FFT is used to demodulate the data in OFDM. The simultaneous and easy computation is made possible by table preparation which has the calculate twiddle factor in it. The number of points in the FFT will dominate the twiddle table. The FFT computation time is reduced by utilizing this table, since there is no need for calculating the factor of run-time. In [28], the subtraction is performed first followed by multiplication in 2-point butterfly structure. The communication process is dominated by the multiplication process and from [29], the IC requirements for implementation of the multiplication process require large area and hardware resources that has greater impact on system power consumption. Hence the FFT is implemented with effective multiplier reduction techniques. The complex multiplication of two numbers, namely R (Real Number) and C (Complex Number) is given by (1).

$$X = RC = (R_r + jR_i)(C_r + jC_i)$$

$$X = (R_rC_r - R_iC_i) + j(R_rC_i + R_iC_r) \quad (1)$$

Four multiplications, one real subtraction and imaginary addition required to compute the FFT from direct architectures as in (1), on the other hand, the (2) reveals the resources requirements after the strength reduction transformation.

$$X_r = (R_r - R_i)C_i + R_r(C_r - C_i),$$

$$X_i = (R_r - R_i)C_i + R_i(C_r + C_i) \quad (2)$$

From (2), one multiplication is reduced at the expense of one adder and two subtractor.

5. Implementation of Discrete Wavelet Transform (DWT)

The small portion of continuous signal bounded by lower and upper limits forms the wavelet. The discrete sampled function of DWT provides the information on both domains namely, Time and Frequency domain. The wavelet transform should possess reconstruction and orthonormal property to adopt it in OFDM. This transform will apply the wavelet function on the signal to form the decomposed signal. Both, low pass filter and high pass filter are presented in Discrete Wavelet Transform (DWT) for decomposing the input signal at each level. The coefficients of high pass filter and low pass filter is called as approximate coefficients and detailed coefficients. Initially the input signal is passed through the low pass and a high pass filter and the coefficients at each level are shown in Fig. 3.

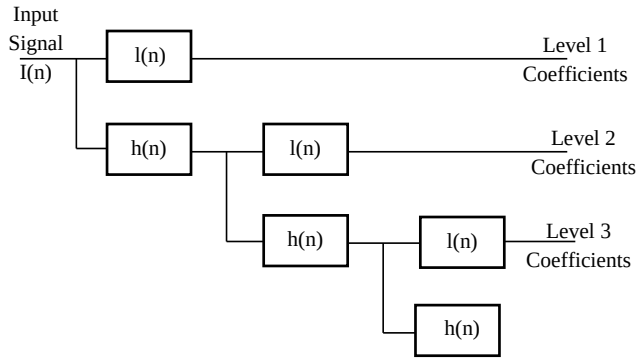

Fig. 3. Decomposition of Signal.

The decomposition of the signal I(n) by wavelet transform can be expressed as in (3) & (4). (3) shows the decomposition of the signal I(n) by a high pass filter and (4) shows the decomposition of the signal I(n) by a low pass filter.

$$W_h(k) = \sum_{n=0}^{\infty} I(n)\, h(2k-n) \quad (3)$$

$$W_l(k) = \sum_{n=0}^{\infty} I(n)\, l(2k-n) \quad (4)$$

Again the level of decomposition is limited by assigning the minimum value of the 'k' and 'n'. The value in the register is changed to increase the level of coefficients. Here, we assume k=1 and n=0 to 1. Then (3) and (4) can be expressed as,

$$W_h(k) = \sum_{n=0}^{\infty} I(n)\, h(2k-n) \quad (5)$$

$$W_h(k) = \sum_{n=0}^{1} I(n)\, h(2-n) \quad (6)$$

$$W_h(k) = [I(0) * h(2)] + [I(1) * h(1)] \quad (7)$$

The equation (7) signifies the decomposed signal I(n) by a high pass filter and similarly the decomposed signal from low pass filter is expressed in (8),

$$W_l(k) = \sum_{n=0}^{\infty} I(n)\, l(2k-n) \quad (8)$$

$$W_l(k) = \sum_{n=0}^{1} I(n)\, l(2-n) \quad (9)$$

$$W_l(k) = [I(0) * l(2)] + [I(1) * l(1)] \quad (10)$$

The proposed architecture developed for (2), (7) and (10) is to implement the Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT) for the reconfigurable Orthogonal Frequency Division Multiplexing (OFDM).

6. Architecture of PE for FFT and DWT

Fig. 4 shows the requirements of resource and Processing Elements (PE) required for the realization of Fast Fourier Transform (FFT). In similar, the resource and PE requirements for the realization of Discrete Wavelet Transform (DWT) is shown in Fig. 5. Both transformation techniques will be reconfigured among themselves in Orthogonal Frequency Division Multiplexing (OFDM). In the reconfigurable OFDM both FFT and DWT shares one adder/subtractor unit.

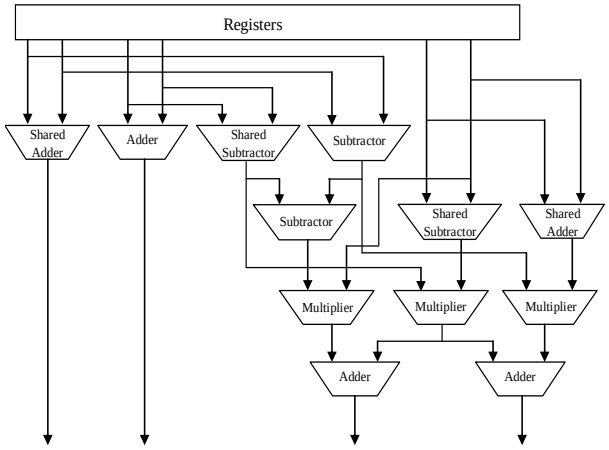

Fig. 4. Fast Fourier Transform (FFT) Architecture for OFDM.

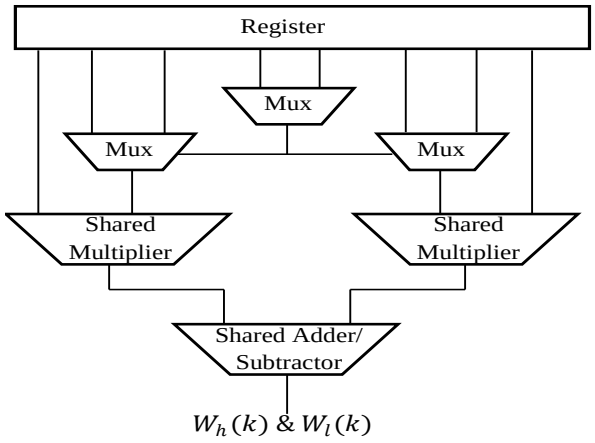

Fig. 5. Discrete Wavelet Transform (DWT) Architecture for OFDM.

The Fast Fourier Transform (FFT) architecture [25], resource utilization is computed as 3 multipliers, 3 multiplexers, 5 adders and 4 subtractors. In similar the proposed architecture of Discrete Wavelet Transform (DWT) for Orthogonal Frequency Division Multiplexing (OFDM) utilizes 3 Multiplexer, 2 shared multiplier and 1 adder/subtractor unit. The shared multiplier in our proposed work will share the multiplier among the low pass and high pass computation of the decomposed signal. This shared multiplier will not take place among the FFT and DWT. To implement (7) and (10), a total of 4 multipliers and two adders/subtractors are required, by our proposed architecture 2 multipliers and 1 adder/subtractor is reduced at the cost of 2 multiplexers. Apart from this the 1adder/subtractor utilized in the proposed architecture will share the resource from Fast Fourier Transform (FFT).

7. Evaluated result

The proposed architecture was developed using Verilog HDL language and simulated using ModelSim, then the developed architecture is mapped into the target FPGA (xc5v1x30ff324) for synthesize analysis. The application mapping is customized as shown in [25] (Fig. 8). The resource utilization of the Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT) is shown in Table 1. Since the computation complexity is low in Fast Fourier Transform, a total of 12440 Gate Element (GE) is consumed by FFT, whereas the proposed reconfigurable Discrete Wavelet Transform (DWT) occupies a total of 14835 Gate Elements (GE). In similar 1282 and 1563 sliced LUT are consumed by Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT) respectively.

Table 1. Resource utilization of FFT and DWT.

Resource Utilization		
Resources	Fast Fourier Transform (FFT) [25]	Discrete Wavelet Transform (DWT)
# Slice LUTs	1282	1563
# Gate Count	12440	14835

The proposed reconfigurable Orthogonal Frequency Division Multiplexing (OFDM), occupies a total of 13651 Gate Elements (GE) with the shared resources, whereas the count is more than the doubled value, when the Gate Element (GE) is computed without the shared resources (i.e. 31783). Likewise, the sliced LUT is reduced when compared with the shared resource. In similar the reconfigurable Discrete Wavelet Transform architecture (DWT) consumes 14835 Gate Elements (GE), the computation is made by considering the 2 shared multipliers in the architecture (Fig. 5).

Table 2. Computation based on Shared Resource.

Resources	Proposed Architecture with resource sharing	Proposed Architecture without resource sharing
# Slice LUTs	1341	3245
# Gate Count	13651	31783

Table 3. PAPR for Various Architecture.

Reference	PAPR (dB)
[30]	7.950
[31]	6.847
[32]	6.828
[33]	11.800
Proposed System	5.573

The total gate count for the DWT will vary if the multiplier is not shared, since the multiplier consumes large area. The proposed architecture with shared resources saves 58.67% and 57.05% sliced LUT and Gate Element (GE) respectively. The proposed reconfigurable Discrete Wavelet Transform (DWT) architecture consumes 16.14% of more Gate Elements (GE) than Fast Fourier Transform (FFT). In similar the 18% of more sliced LUT is consumed by proposed architecture when compared to the FFT. The Peak-to-Average-Power Ratio (PAPR) is realized for various architectures of OFDM, as shown in Table 3.The proposed architecture achieves a PAPR of 5.573dB, which is low compared to various architecture.

8. Conclusion

The reconfigurable Orthogonal Frequency Division Multiplexing (OFDM) is proposed in this paper. The proposed OFDM will configure between Fast Fourier Transform (FFT) and Discrete Wavelet Transform (DWT) based on the application needs. The reconfigurable OFDM is developed using Verilog HDL and targeted in Xilinx Virtex 5 FPGA (xc5v1x30ff324). The proposed OFDM shows a performance improvement in terms of Peak-to-Average-Power Ratio (PAPR) with slight area overhead. The proposed OFDM saves 58.67% and 57.05% sliced LUT and Gate Element (GE) respectively (with shared resources). Also the proposed OFDM achieves a Peak-to-Average-Power Ratio (PAPR) of 5.573 dB. In future the idea can be expanded to reduce the PAPR and area overhead.

"Compliance with Ethical Standards"

1. Disclosure of potential conflicts of interest

The authors not having conflicts of interest.

2. Research involving Human Participants and/or Animals and Informed consent

Not applicable.

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