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Electrical and dielectric properties of Au/SiO_2/n-GaAs (MOS) structures with different oxide layer thickness

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The electrical and dielectric characteristics as series resistance (R_s), dielectric constant (εə), dielectric loss (ε∀) and dielectric loss tangent (tanδ) of the Au/SiO_2/n-GaAs (MOS) structures with different oxide thickness have been investigated in room temperature at 1 MHz. Applied voltage and oxide thickness dependence of these structure investigated by using experimental capacitance (C) and conductance (G/*w*) measurements in the applied voltage (-3 to 1,5 V) and oxide thickness (130-240 Å) range. Experimental results show that, while the capacitance values decrease with increasing oxide layer thickness, series resistance values increases. Also the change in G_m/w curves with interfacial oxide layer thickness is slight. While the capacitance values decrease parabolic with increasing interfacial oxide layer thickness the series resistance values increase linearly. The εə values decreases rapidly at above 1 V, ε∀ and tanδ decreases rapidly.

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1. Introduction

In semiconductor technology, metal-semiconductor (MS) contact is used rectifying contact mostly. These devices are converted the metal-oxide-semiconductor (MOS) devices by an interfacial oxide layer which is constituted between metal and semiconductor. The MOS structures constitute a kind of capacitor, which stores the electric charge virtue of the dielectric property of interfacial oxide layer. The interfacial oxide layer may cause interface state charges with bias due to an additional electric field in the insulator layer and influence the both electrical and dielectric characteristics [1-10]. The electronic states associated with the surface region were called interface traps or surface states. The reason of their existence is the interruption of the periodic lattice structure at the surface [1-3], surface preparation, dangling bonds at the semiconductor surface, surface formation of insulating layer and impurity concentration of semiconductor. When a voltage is applied the MOS structure, the voltage is shared by interfacial oxide layer, depletion layer and series resistance (R_s) of the structure. And the magnitude of this shared voltage depends on insulator layer thickness and R_s. Therefore, the performance and reliability of these devices are especially dependent on formation of insulator layer at M/S interface.

This interfacial insulator oxide layer thickness is very important parameter for this MOS structures. If the oxide layer is thin, although the capacitance is higher sometimes the leakage current can occurs between metal and semiconductor. This situation which is not required constitutes some problem on the device reliability and yield. Otherwise a thick interfacial oxide layer doesn't permit the current between metal and semiconductor but MOS capacitance decreases. This cause the interfacial oxide layer thickness must be optimum value.

The capacitance and conductance measurements give the important information on electrical and dielectric characteristics of the MOS structure. In order to achieve a better understanding of the effects of interfacial oxide layer thickness, we measured the capacitance (C) and conductance (G/w) as a function of voltage for MOS structures with different oxide layer thickness. In this study, electrical and dielectric properties of Au/SiO_2/n-GaAs (MOS) structures have been investigated by capacitance (C) and conductance (G/*w*) measurements technique in room temperature at 1 MHz. To determine the dielectric constant (ε'), dielectric loss (ε'') and loss tangent (tan δ) of MOS structure, the admittance technique was used [1,11].

2. Experimental method

Au/SiO_2/n-GaAs (MOS) structures were fabricated on the 5.08 cm diameter float zone (100) n-type GaAs wafer having thickness of about 350 μm with 2-3x10^{18} cm^{-3} carrier concentrations. For the fabrication process, the firstly GaAs wafers were dipped in ammonium peroxide for a few seconds to remove native oxide layer on the surface. Au/Ge/Ni alloy was evaporated onto the whole back side of the wafer at a pressure about 10^{-7} Torr in a vacuum system. In order to perform the ohmic contact, wafer was sintered at 430 ^oC for 40 seconds. Insulator layers (SiO_2) with different thickness were coated on the upper surface of the GaAs by using PECVD technique. In PECVD system SiH_4 gas was used for Si source and O_2 gas used for oxygen source. The wafer was placed in the vacuum system after SiO_2 coated high purity gold (Au)

front/Scottky contacts with a thickness of 1500 Å were evaporated at a rate of ~on the 2 Å/s through a metal shadow masks with circular dots of 1 mm diameter. The metal layer thickness and the deposition rates were monitored with the help of quartz crystal thickness monitor. The interfacial insulator layer (SiO_2) thicknesses were estimated to be about 130, 163 and 240Å from measurement of the insulator capacitance (C_{ox}) in the strong accumulation region at 1 MHz.

The capacitance-voltage (C-V), and conductance-voltage (G/w-V) characteristics of Au/SiO_2/n-GaAs (MOS) structures were measured in the applied voltage range of -3-1,5 V at room temperature. The C-V and G/w-V measurements were performed by using HP 4192A LF impedance analyzer (5 Hz–13 MHz) and the test signal of 40 mV_{rms}.

3. Results and discussion

In this work, electrical characteristics as capacitance (C_m), conductance (G_m/w), serial resistance (R_s) and dielectric properties as dielectric constant (ε'), dielectric loss (ε'') and dielectric loss tangent (tanδ) of Au/SiO_2/n-GaAs (MOS) structures with different oxide layer thickness have been investigated at room temperature to observed these main structure parameters at 1 MHz. There are three MOS structures with different oxide thickness; M1, M2, M3, with 130, 163, 240 Å oxide thickness, respectively.

3.1. Electrical characteristics

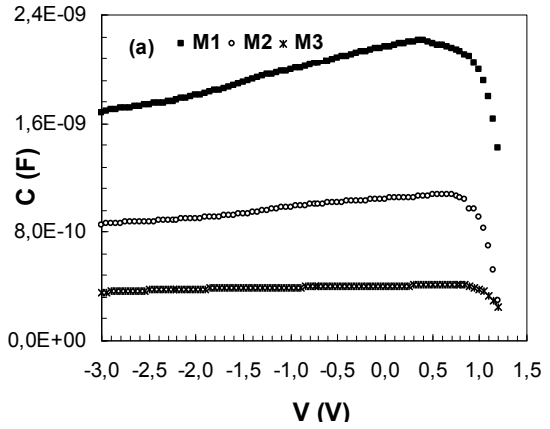
The capacitance-voltage, conductance-voltage and series resistance-voltage versus of Au/SiO_2/n-GaAs with different oxide thickness structures are shown in Fig. 1(a), (b) and (c), respectively.

The series resistance of these MOS structures can be obtained from the measurements of C_m and G_m/w data. Series resistance (R_s) can be obtained as [12,13]

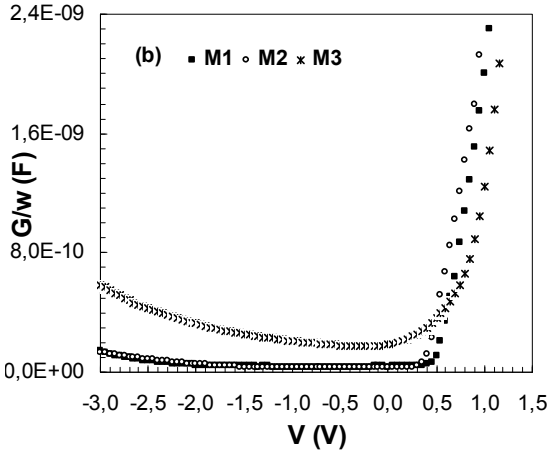
$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \qquad (1)$$

where C_m and G_m is the measured capacitance and conductance.

Fig. 1(a) and (b) shows the measured capacitance-voltage (C-V) and conductance-voltage (G/*w*-V) characteristics and (c) series resistance of these structures at room temperature. It is clear that while the capacitance and conductance is changes slightly depend on bias voltage these values very sensitive to interfacial oxide layer thickness. As shown in Fig. 1; while the capacitance values decrease with increasing oxide layer thickness, series resistance values increases. Also the change in G_m/w curves with interfacial oxide layer thickness is slight. The series resistance changes slightly in negative bias voltage region and give a peak in positive bias voltage region. This peak position shifts towards to negative bias region. The series resistance peak values 40.92; 73.86; 191.86 Ω at 1.10; 0.80; 0.55 V for M1, M2, M3 respectively.



(a)



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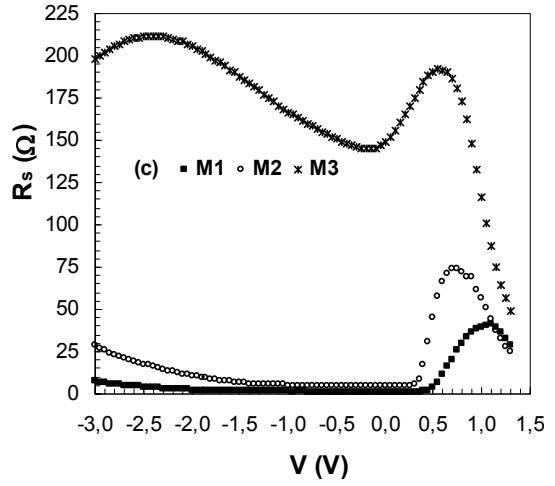
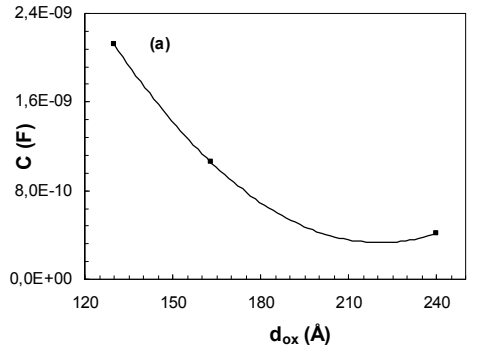


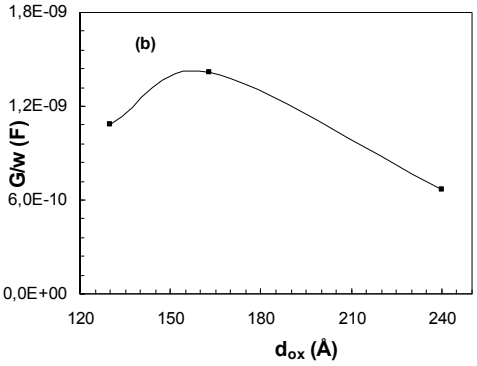
(c)

Fig. 1. (a) capacitance-voltage, (b) conductance-voltage and (c) series resistance-voltage versus of M1, M2 and M3.

Fig. 2(a), (b) and (c) shows the interfacial oxide layer thickness dependence of the C, G/*w* and R_S characteristics of these structures at room temperature. While the capacitance values decrease parabolic with increasing interfacial oxide layer thickness the series resistance values increase linearly. This linear increase in the values of series resistance in accumulation region (0,8 V) is the same behavior with conductor. This situation may be attributed to dielectric strength of SiO_2 in accumulation region because of breakdown field can be as low as 10^6 V/cm in PECVD oxides.



(a)



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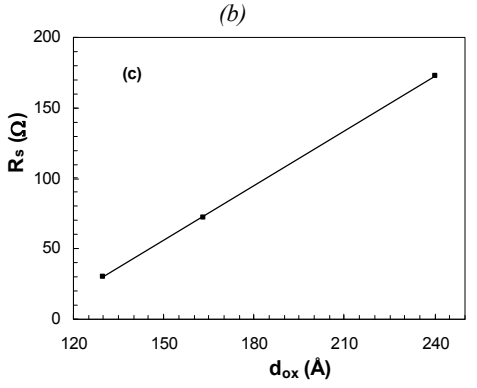


(c)

Fig. 2. (a) capacitance-oxide thickness, (b) conductance-oxide thickness and (c) series resistance- oxide thickness versus of M1, M2 and M3 at room temperature.

3.2. Dielectric properties

The values of the ε' and ε" at different temperatures were obtained from the measured capacitance (C_m) and conductance (G_m/w) as following equations, respectively [14,15].

$$\varepsilon' = \frac{C_m d_{ox}}{\varepsilon_o A} = \frac{C_{ox}}{C_o}$$

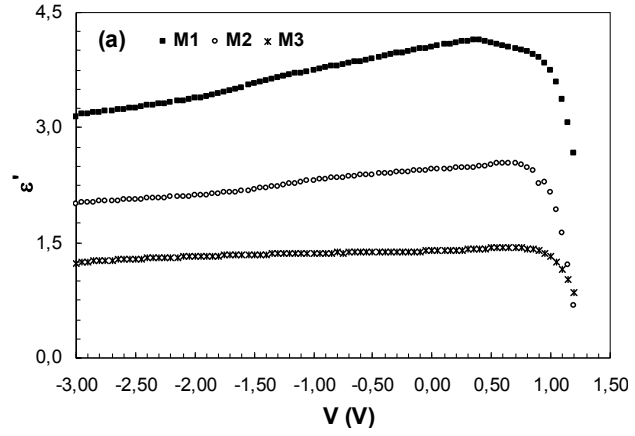
$$\varepsilon'' = \frac{G_m d_{ox}}{\omega \varepsilon_o A} = \frac{G_m}{\omega C_o} \qquad (2)$$

where; C_o is the equivalent capacitance of the free space, A is the area of the sample, d_{ox} is the interfacial insulator layer thickness, ε_o is the permittivity of free space charge (ε_o = 8.85x10^{-14} F/cm) and ω (=2πf) is the angular frequency.

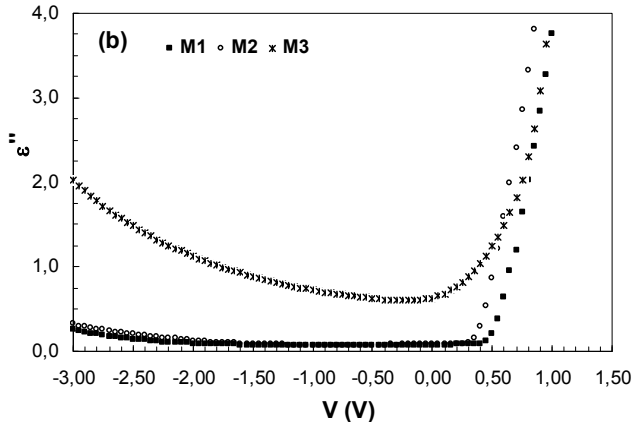
Additionally, the values of loss tangent (tanδ) can then the obtained from the ratio of the imaginary part to the real part of dielectric constant (ε"/ε'), or from the measured C_m and G_m [14].

$$\tan(\delta) = \frac{G_m}{\omega C_m} = \frac{\varepsilon''}{\varepsilon'} \qquad (3)$$

Fig. 3 (a), (b) and (c) shows the values of ε', ε" and tanδ of M1, M2 and M3 (MOS) structures as a function of bias voltage. It is clear that while the ε' increases slightly with increasing bias voltage at negative voltage region, ε" and tanδ decreases. The ε' values very sensitive to interfacial oxide layer thickness. As shown in Fig. 3; while the ε' values decreases rapidly at above 1 V, ε" and tanδ decreases rapidly. Especially while M3 MOS structure that has the thickest oxide layer dielectric behavior (ε') is stable dielectric loss and loss tangent behavior is changeable the others. In this case we say that, while the interfacial oxide layer thickness becomes thick dielectric behavior (dielectric constant) of this structure become stable.



(a)



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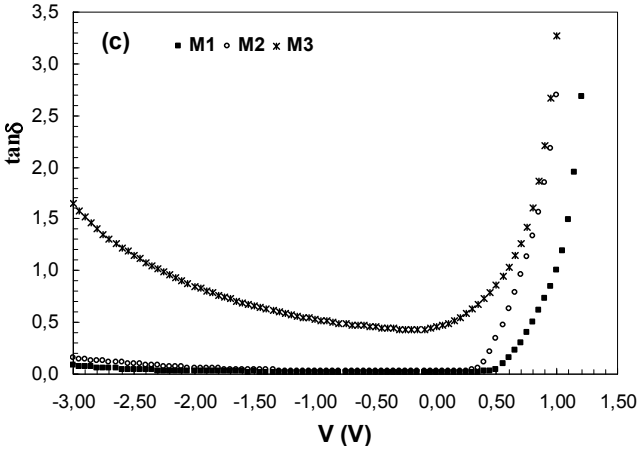
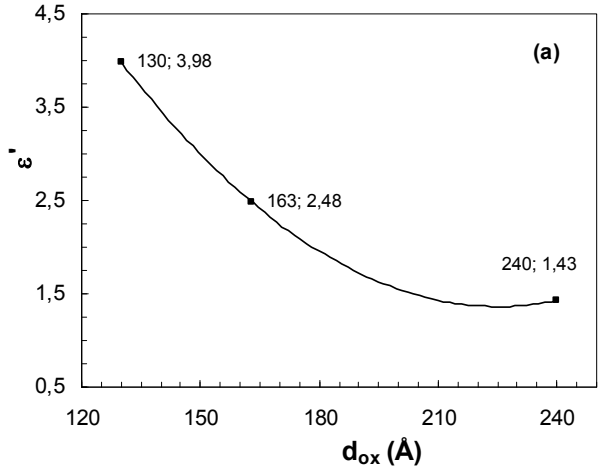


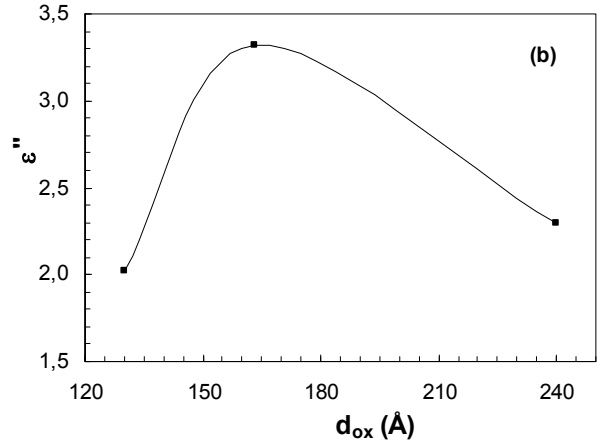
(c)

Fig. 3. (a) Dielectric constant (ε')-voltage, (b) dielectric loss (ε'')-voltage and (c) loss tangent (tanδ)-voltage versus of M1, M2 and M3.

Fig. 4 (a), (b) and (c) shows the values of ε', ε'' and tanδ as a function of interfacial insulator layer at room temperature. As shown in Fig. 4, while the ε' values decrease parabolic with increasing interfacial oxide layer thickness tanδ values increase parabolic with increasing interfacial oxide layer thickness. Also ε'' versus have a peak for the thickness values of 163 Å.



(a)



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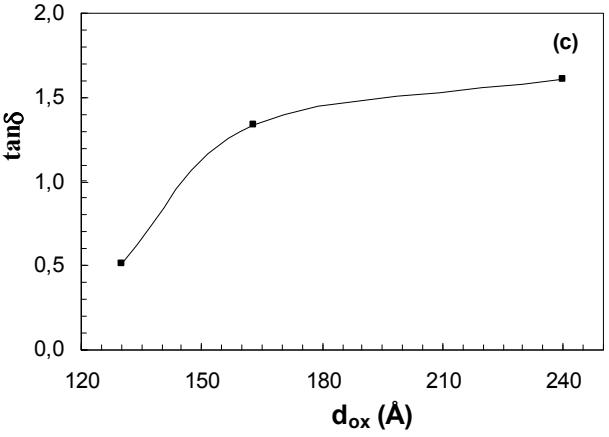

(c)

Fig. 4. (a) Dielectric constant (ε')-oxide thickness, (b) dielectric loss (ε'')-oxide thickness and (c) loss tangent (tanδ)- oxide thickness versus of M1, M2 and M3 at room temperature.

4. Conclusions

In this work, capacitance (C), conductance (G/*w*), series resistance (R_S) and dielectric properties of Au/SiO_2/n-GaAs (MOS) structures have been investigated at room temperature in order to good interpret to observed some main structure parameters such as the R_s, εə, ε∀ and tanδ at 1 MHz. It was seen that, the electrical and dielectric parameters of these structures very sensitive to interfacial oxide layer thickness. The C and ε' values are almost bias voltage independent contrary to these values decrease parabolic with increasing interfacial oxide layer thickness. Also, while the capacitance values decrease parabolic with increasing interfacial oxide layer thickness the series resistance values increase. The change in G_m/w curves with interfacial oxide layer thickness is slight. The εə values decreases rapidly at above 1 V, ε∀ and tanδ increase rapidly.

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