Synthesis and characterization of nanostructured CdS:Cu thin films prepared by CBD for diode applications

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Nanostructured cadmium sulfide doped by copper (CdS:Cu) thin films were deposited on glass and wafer silicon by chemical bath deposition method. The prepared thin films were annealed at 250 ^{o}C at different times (30, 60, and 90 min). The structural properties of the samples were characterized using X-ray diffraction (XRD), and the crystalline size of the CdS:Cu thin films was calculated from XRD data. All samples had a polycrystalline structure, and annealing time increased the crystalline size. Field emission scanning electron microscopy of the morphology of the CdS:Cu thin films revealed the presence of nanoparticles with grain sizes ranging from 71.52 nm to 26.55 nm after 90 min of annealing. Moreover, CdS:Cu thin films were deposited on an n-type silicon substrate to prepare a CdS:Cu/Si junction, and the effects of annealing time on the electrical properties of this junction were investigated. The current density-voltage (J-V) characteristics were studied, and the results revealed that the CdS:Cu/Si junction had an ideality factor (n*) of 1.381 and a saturation current (J_s) of 0.007 mA/cm^2, which increases with increasing annealing time. However, the potential barrier (Φ_b) and the rectification factor (R_f) decreased with increasing annealing time, indicating a trade-off between conductivity and R_f due to substantial changes in the electrical transmission mechanisms.

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1. Introduction

Micro- and nano-electronics widely use cadmium sulfide. In particular, p-n junction applications, such as diodes and photo-electric converters for solar energy, are an important area of CdS application [1]. As with most substances, their properties change significantly during the transition from a bulk to a nanostructured state [2]. Thus, when the size of a CdS nanoparticle decreases to range (100 to 10) nm, the band gap increases from 2.5 to 4.5 eV [3]. This opens up new possibilities for utilizing nanostructured CdS optical properties in the visible and ultraviolet ranges of the optical spectrum. For example, CdS thin films are a promising material as a "window layer" for CIGSSe solar cells [4, 5]. Due to the nonlinear dependence of the frequency of luminescent radiation on the particle size, CdS nanoparticles can serve as quantum dots for visualizing biological objects and developing new optoelectronic devices. To investigate exactly how the electrical properties of CdS nanoparticles change with their size, it is essential to characterize the structure of CdS in its nanostate. This will facilitate their use in technology [6, 7]. Accurate knowledge of the structure will enable the determination of potential forms of nano-CdS, enabling the creation of new materials such as hybrid core-shell structures or colloidal crystals. The size and shape of a nanoparticle can also significantly affect its electronic properties, and a single defect due to the particle's smallness can completely determine its structure. Therefore, precision is required and must be taken when determining and examining the structure, size, and shape of nanoparticles [8, 9]. It is important to note that both laboratory and industrial settings can produce various forms of nanostructured CdS without the need for special equipment. Several methods are used to form CdS thin films, including molecular beam epitaxy, deposition from metal-organic compounds in a phase, sublimation in a closed volume, pyrolysis of aerosols, electrochemical precipitation, and precipitation in a chemical bath from aqueous solutions [10, 11]. Despite the large number of publications dedicated to the study of CdS, the task of optimizing the technology for its production research and the study of heterostructure characteristics remains relevant [12]. According to previous studies and published literature, pure CdS is n-type. Therefore, it can be doped with silver Ag or copper Cu to transform it into a p-type semiconductor. Copper is an important element in scientific applications due to its high electrical conductivity, it is widely used in electronic devices and advanced scientific instruments [13, 14]. When CdS films

are deposited on wafers of silicon (as substrates), a CdS/Si junction is obtained. The diode junction was prepared using n-type silicon wafers and p-type CdS thin films. The difference in work functions between Si and CdS forms a voltage barrier and depletion region, leading to differences in the behavior of the current passing through this junction at both forward and reverse bias. Applications such as rectifiers, mixers, and high-frequency devices, among others, can utilize CdS/Si diodes [15, 16]. Research aims to prepare a CdS:Cu/Si junction and study the effect of annealing time on it. The objective is achieved by preparing nanostructured thin films of CdS doped by Cu to obtain a p-type semiconductor using the chemical bath method and then studying and determining their structural and morphological properties. These thin films deposited were on n-type silicon wafers to create a CdS:Cu/Si junction. These samples are being annealed at different times to study the effect of annealing time on the properties of the hybrid junction, with a focus on changing the electrical and structural properties by increasing the annealing time.

2. Experimental

The following components were made into aqueous solutions to create CdS:Cu thin films: 8 mL of NH_3 solution, 4 mL of 0.02M NaOH, 4 mL of 0.1M $CdCl_2$, and 8 mL of 0.05M $CS(NH_2)_2$. 4 mL of 0.01M $CuCl_3.6H_2O$. All solutions were combined and added with distilled water to obtain a total of 50 mL. The Cu doping concentration was 10 mol% relative to Cd. The pH of the final solution was measured and was approximately 10-11. The glass and wafer n-Si substrates were inserted and suspended vertically in solution, which was subjected to constant stirring for 3 h. The substrate, which had an orange-yellow coating, were removed, cleaned with distilled water, and air dry. The prepared films were annealed at 250 °C for varying durations (30, 60 and 90 min). Thin films deposited on glass were used for structural and morphological testing and thickness measurement, and those deposited on Si wafers were used for diode fabrication. An X-ray diffractometer (Phillips Xpert model) was used to conduct X-ray diffraction (XRD) to verify the structural characteristics of the samples. The samples were morphologically analyzed through field emission scanning electron microscopes (FE-SEM; TESCAN MIRA3). Hall effect measurements were conducted to evaluate the conductivity type (n-type or p-type) of the prepared samples. A test was also performed to study the J-V at forward and reverse biases after silver paste electrodes were placed on both sides of the CdS:Cu/Si junction. The thickness of the films t was measured using the optical interference method. This method relies on the interference of light beam reflections from the surface of the thin film and substrate. A helium-neon laser (0.632 μm) was used, and the thickness was determined using the following formula:

$$t = \frac{\Delta x}{x} \frac{\lambda}{2} \quad (1)$$

where: x is the fringe width, Δx is the distance between two consecutive fringes, and λ is the wavelength of the laser light. The thickness of the prepared films was found to be around 543±15 nm.

3. Result and discussion

The morphology of the obtained samples was studied by FE-SEM. Fig. 1 shows the FESEM images of as-synthesized CdS:Cu and annealed thin films at different temperatures. The surface of the as-synthesized CdS:Cu thin film had some irregular semi-spherical nanoparticles clumped together. The grain sizes were between 71.52 and 77.14 nm, and some large plate-shaped clusters were found. These plates disappeared, the aggregation sizes increased, and the nanoparticle sizes decrease to 65.56 and 63.75 nm when the thin films were annealed for 30 min. Annealing CdS:Cu thin films for 60 min substantially altered their morphology, resulting in a uniform distribution, consistent shape, and a reduction in their grain sizes to 50.11 and 46.67 nm. Annealing for 90 min leads to a continued decrease in the grain sizes of the nanoparticles (reaching 33.87 and 26.55 nm) and their return to agglomeration. Some particles mergedto form a nanorod-like structure.

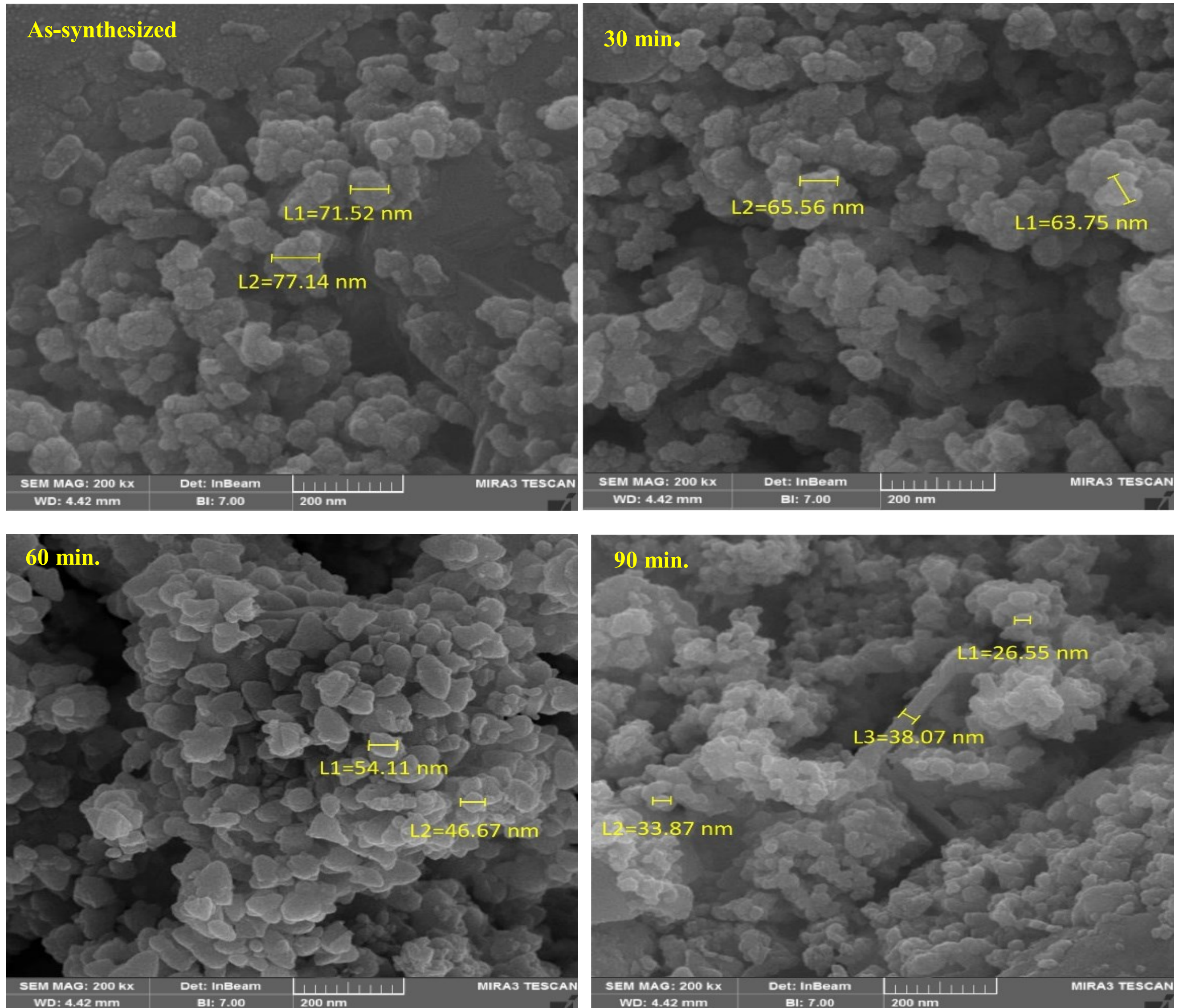


Fig. 1. FE-SEM images of CdS:Cu thin films at different annealing times (colour online)

Fig. 2 displays the XRD patterns for the CdS:Cu thin films, which were prepared using a chemical bath technique and annealed at various times (0, 30, 60, and 90 min). The patterns indicate the polycrystalline structure of the prepared CdS:Cu thin films, where many peaks were observed [17]. Comparison with standard data from the JCPDS card (File No. 41-1049) showed that CdS:Cu existed in a mix of cubic and hexagonal phases, and hexagonal ones were dominant [18]. The major peaks corresponded to hexagonal phases at $2\theta = 23.6^o$, 26.7^o, 28.3^o, 43.9^o, and 48.8^o for (100), (002), (101), (110), and (103), respectively. The minor peaks corresponding to values of $2\theta = 45.6^o$ and 52.1^o for (220) and (311), respectively, suggests the presence of a cubic phase. Furthermore, some peaks were not phase-specific and may be impurities from the reacting chemicals. This assertion was confirmed by the disappearance of these peaks after increasing the annealing time. Calculation of the crystalline size of the prepared samples basis of the Scherrer equation [19], ($D = 0.9\lambda/B \cos\theta$), where D is the crystalline size, 0.9 is a constant, λ is the wavelength of x-ray, B is the full width at half maximum, and θ is the Bragg angle. The results revealed that the crystalline size increases with increasing annealing time (Table 1), indicating an improvement in the crystalline state with increasing annealing time.

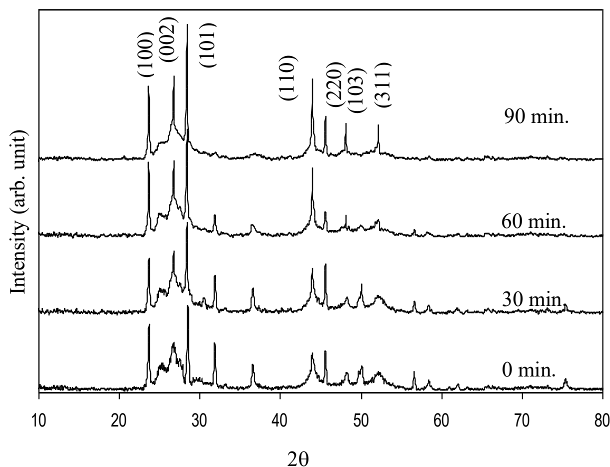


Fig. 2. The XRD spectra of CdS:Cu thin films for different annealing times PANI/f-SWCNT thin films

According to the results above, the increase in crystalline size did not contradict the increase in annealing time and the decrease in the apparent grain size in FE-SEM images. Grain size represents the surface agglomerates of multiple crystallines, and the Scherrer equation represents the size of the crystals in the coherent diffraction domain size. Therefore, the annealing process improves crystallinity and reduces agglomeration, leading to enlargerd crystalline grains.

The Hall measurements results indicate that all samples were p-type, with charge carrier concentrations of 6.34×10^{13}, 2.34×10^{14}, 5.76×10^{14}, and 9.83×10^{14} cm^{-3} for as-synthesized CdS:Cu thin films and annealed at 30, 60, and 90 min, respectively.

The J-V curve graphically expresses the current density-voltage characteristic of a p-n junction and depends on the current flow through the junction. The J-V can be linear and nonlinear and can be employed identify the characteristics of the manufactured junction. When the voltage applied to a CdS:Cu/Si junction increases, the current density in it increases much faster than the voltage does (Fig. 3).

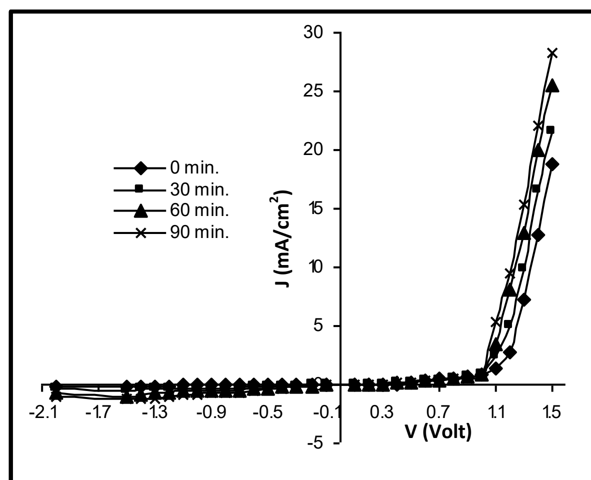
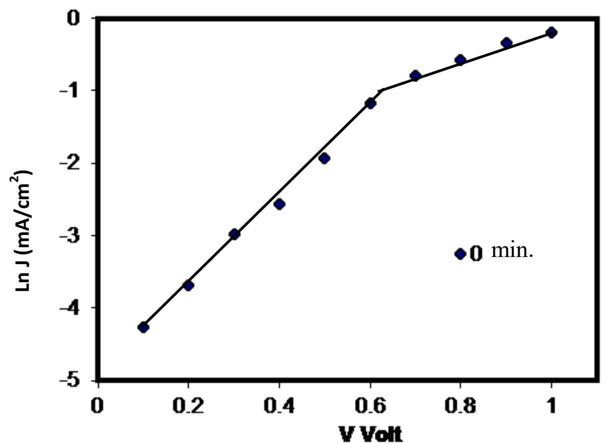
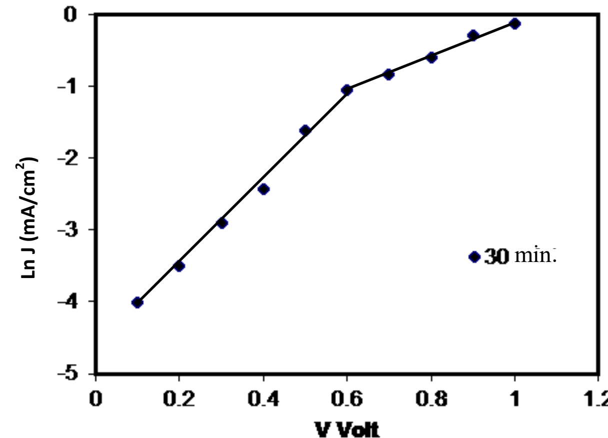
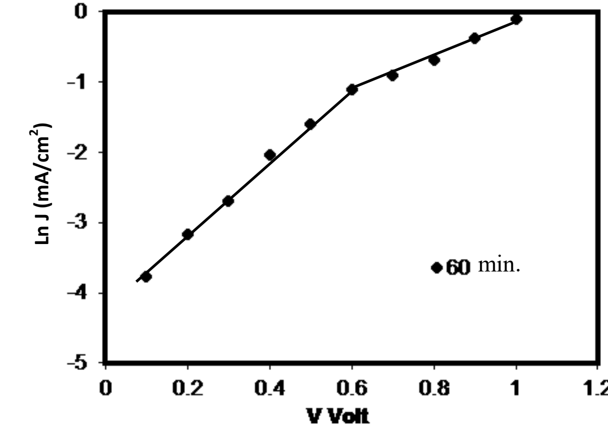


Fig. 3. Current density -Voltage characteristics of CdS:Cu/Si for different annealing times







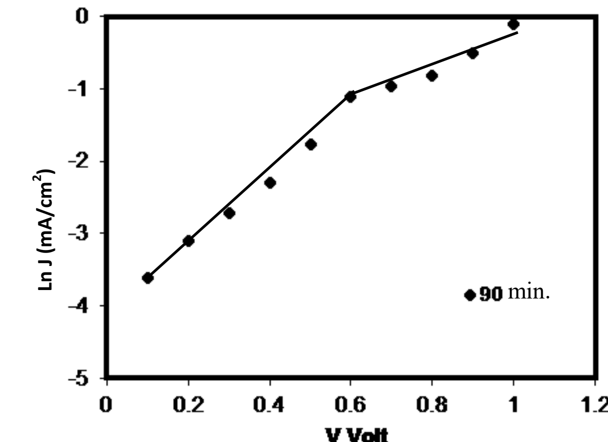


Fig. 4. Characteristics of the ln J-V at the forward bias of the CdS:Cu/Si junction at different annealing times

This phenomenon means that the relationship between current and voltage is nonlinear. If the voltage changes to the opposite (-V) and the current density-voltage changes in the junction have the same character, then such a junction exhibits a symmetrical J-V characteristic, However, in a CdS:Cu/Si junction, because the different types of materials (n-type and p-type) have an asymmetrical J-V characteristic, when exposed to (-V), the CdS:Cu/Si system does not pass current in the reverse direction. A very small amount of current density (J_{rev}) flows through the p-n junction because the presence of minority current carriers in the semiconductors (electrons in a p-type semiconductor and holes in an n-type semiconductor). The reason for this is the high resistance of the transition layer (p-n junction) that appears between the p-type semiconductor and the n-type semiconductor.

Moreover, with the increase in annealing time, the forward current density increased, and rectification factor R_f decreased (Fig. 3 and Table 1). These results may be attributed to the improvement in the crystal structure resulting from the increase in crystalline size, which led to an increase in the reverse leakage current and a decrease in the Φ_b. The J_s of the CdS:Cu/Si junction can be derived by plotting the forward bias voltage and current density (lnJ) and taking the intercept along the y axis (Fig. 4) in the first region.

The saturation current density increased as the annealing time increased (Table 1). This trend is consistent with the observed decrease in the Φ_b. Given that the annealing process improves crystallinity and increases crystalline size, the effective Φ_b at the junction decreases, leading to an increase in the saturation current density in accordance with the thermal emission model [20, 21]. The ideality factor n* for the prepared CdS:Cu/Si junction was calculated using the equations below [22, 23]:

$$\ln J = \ln Js + \left(\frac{qV}{n^* K_B T} \right). \quad (2)$$

$$n^* = \frac{q}{K_B T} \left[\frac{d\left(\ln\left(\frac{J}{Js} \right) \right)}{dV} \right]^{-1}. \quad (3)$$

where q is the electron charge and K_B is the Boltzmann constant. Table 1 shows that the n* increased with increasing annealing time. This change is due to the fact that despite the improvement in crystal structure and the increase in crystalline size, the current transfer mechanism changed because of the recombination-generation process at the interface or grain boundaries. This pattern is consistent with the J_s results. Conversely, excessive annealing times may lead to a deterioration of the material's properties, necessitating careful optimization. The barrier height Φ_b was calculated using the equations below [22].

$$J_s = A^* T^2 \exp\left(\frac{q\Phi_b}{K_B T} \right). \quad (4)$$

where A* is Richardson's constant. Table 1 shows that the value of the Φ_b for CdS:Cu/Si junction decreased with annealing time because annealing improving the CdS:Cu and Si bonds, enhanced the crystal structure and reduces the defects in CdS:Cu. This process created minimal contamination and imperfections that could restrict the energy transfer between the two layers of the junction.

The tunneling constant A_t can be determined depended on Fig. 4 and the equation [24]

$$A_t = \left[\frac{d \ln(J_f / J_s)}{dV} \right]. \quad (5)$$

where If is the forward current density taken from the linear region (a) of the ln J-V plot, J_s the saturation current density for this region. and the values of A_t and the effect of annealing temperature time on it are listed in Table 1.

Table 1. The crystalline size of CdS:Cu thin films and electrical parameters of CdS:Cu/Si junction

T_a time (min.)	Crystal size (nm)	J_s (mA/cm^2)	R_f	n*	Φ_b eV	A_t
0	28.55	0.007	81	1.381	0.572	20.73
30	33.58	0.010	46	1.404	0.567	24.58
60	42.82	0.013	26	1.589	0.559	27.80
90	53.52	0.018	27	1.681	0.550	28.96

4. Conclusion

The study concludes that a CdS:Cu/Si junction can be successfully prepared using the chemical bath deposition method, and annealing at different times changes the material's structural and electrical properties. Specifically, an improvement in the crystal structure was observed, as evidenced by the crystalline growth from 28.55 nm to 53.52 nm and the decrease in crystal defects. This crystalline improvement was supported by the increase in charge carrier concentration with increasing annealing time, as demonstrated by Hall measurements. These changes led to a decrease in Φ_b and a rise in J_s in accordance with the thermal emission model. However, n* increased from 1.381 to 1.681 because of the increase in recombination processes. Accordingly, the R_f values decreased because of the increase in leakage current. This discrepancy between the decrease in R_f and the improvement in conductivity emphasizes the necessity of selecting an intermediate annealing time to achieve ideal results for fabricated diodes.

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