Taguchi optimization of a SOI-based lateral PIN photodiode using SiGe/Si multilayer quantum well

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Silicon–on-insulator (SOI) based SiGe quantum well infrared pin photodiode has the potential of being a serious candidate for applications in sensing applications as well as in optical fiber communications. The objective of this paper is to optimize the process parameters for a SOI-based lateral PIN photodiode using SiGe/Si multilayer quantum well (MQW) to obtain high responsivity, frequency response, quantum efficiency and low transient time. An L9 array from Taguchi method was used to optimize the device design. Four process parameters were chosen, namely the intrinsic region length, photo-absorption layer thickness, the incident optical power and the bias voltage. Two noise factors i.e. the time and temperature of the n-well diffusion process were also used to make the device design insensitive to variation in selected fabrication parameters. ATHENA and ATLAS module from Silvaco Int. were used for the fabrication simulation and electrical characterization. The results obtained for responsivity, frequency response and transient time after the optimization approach were 0.87 A/W, 20 GHz and 1.75 x 10^{-11} respectively which correspond to the optimization value for the intrinsic region length of 6 µm, photo-absorption layer thickness of 0.505 µm, incident optical power of 0.5 mW/cm^{2}and bias voltage of 3.5 V. As a conclusion, the optimum solution in achieving the desired high speed photodiode was successfully predicted using Taguchi optimization method. The percent of improvement for responsivity and frequency responses are 22.3% and 5.26% respectively.

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Keywords: Taguchi method, Photodetector device, ATHENA, ATLAS

1. Introduction

Optical communication networks, chip-to-chip interconnects, and on-chip optical interconnects have gained widespread interest owing to the inherent advantages of large bandwidth, high performance and reduced power dissipation of optical communication system. Monolithically integrated high speed, low cost, and high efficiency optical receivers on silicon chips are the key components for these applications. With thin layers of Silicon-on-Insulator (SOI), the electrical current leakage that degrades the performance of the device can be reduced. Therefore, SOI substrate was used in this research to develop a photodiode for sensing as well as optical fiber communications applications.

Quantum wells are essentially suitable for infrared photo-detection because of their high sensitivity to normal incidence lights and low dark current [1]. The advantage of using SiGe for optoelectronic devices, include the low defect density of the material, that it can enhance operations even at room temperatures [2]. Also a SiGe-based multi-quantum well device's operating wavelength can be tuned over a range of 1.3 µm to 1.55 µm making them ideal choices for sensing and optical fiber communications [2].

In the literature, SiGe/Si quantum well photodiode were designed with 20 multi quantum wells (MQW) of Ge/Si bilayers and 25 nm of Si spacer layers. The device exhibited responsivity of 0.158 mA/W at 1.31 µm with an applied voltage of 1-V [1]. In previous research [3], the results of frequency response was up to 40 GHz at 1300 nm to 1550 nm. Sood et. al [4] reported at -1V and wavelength of 1550 nm, the 5 x 10 µm device with Ge quantum wells were alternated within 10 nm to 30 nm Si barrier layers and had a responsivity of 0.18 A/W. The photodiode with a SiGe/Si MQW thicknesses of 5 and 25 nm respectively,exhibited responsivity of 0.3 A/W at a small bias of 2V [5].

This paper investigates the optimization of the process parameters on the frequency response and responsivity of a Si lateral pin-photodiode based on the device which was developed previously [6, 7, 8]. A two dimensional model of a SOI-based lateral PIN photodiode operating at the optical wavelength, λ from 400 nm to 1600 nm was developed using an industrial based numerical software [9].

Statistical optimization of the Si SOI-based lateral PIN photodiode model was executed using L_9orthogonal array by using Taguchi optimization method. Taguchi method provide the most efficient and viable solution in such cases with minimal experimental trials. The optimization of design parameters is one of the vital industrial functions to improve the product performance as well as to save manufacturing cost. In previous research [10], Taguchi method was used in the optimization of gate oxide and silicide thickness for 45 nm NMOS device. The optimization method of designing experiments based on Taguchi Methods for optimal solution in producing 32 nm CMOS technology transistor with desired leakage current was also reported [11].

In this work, both numerical modeling and Taguchi optimization was used. Improvement for the quantum efficiency and transient response were obtained from the best setting of the process parameters after the optimization approach. This methodology aids in cost-effective device optimization prior to the actual fabrication of the device.

2. Methodology

The Si lateral pin-photodiode was simulated on a silicon substrate (n^+-type) with thicknesses of 50 µm using ATHENA software from Silvaco Int. Then, the SiO_2 buffer layer was deposited on the Silicon substrate with thickness of 400 nm. In order to fabricate the device, 5 periods of $Si_{0.5}Ge_{0.5}$/Si multi-quantum well were deposited onto the (100) n^+-type Si substrate. The thicknesses of the SiGe with a Ge content of 50% and Si layers are 5 and 20 nm, respectively Then, the n-well was developed using phosphorus diffusion with dopant concentration of 2.02 x 10^{19} cm^{-3} on the left side of the photodiode with diffusion temperature of 1000 ^{0}C for 50 seconds. Whilst the p-well was diffused with boron concentration of 8.09 x 10^{19} cm^{-3} on the other side of the photodiode with temperature of 1000 ^{0}C for 120 seconds. SiO_2 layer with thickness of 280 nm was deposited on the silicon substrate to act as a passivation layer. The electrode contacts with thickness and length of 500 nm and 6000 nm respectively, were processed by depositing aluminum on the n-well and p-well areas of the silicon photodiode.

The responsivity of a pin-photodiode is given by [6]:

$$\mathcal{R} = \frac{I_T}{I_S}\left(\frac{\lambda}{1.24}\right) \tag{1}$$

where I_s is the source photocurrent, I_T is the cathode current and λ is the optical wavelength. Calculation for the total quantum efficiency (%) is given by equation (2) [6] :

$$\eta_{total}\,(\%) = \frac{I_{cathode}}{I_{source\ photo\ current}}.100\% \tag{2}$$

The frequency response is defined as [8] :

$$f_{-3dB} = 20^{*}\log\left(\frac{I_R}{I_{RO}}\right) \tag{3}$$

where I_R is the real cathode current and I_{Ro} is the real component current. Whilst, the transient response, t_r is given by equation (4) [6]:

$$t_r = \frac{0.35}{f_{-3dB}} \tag{4}$$

L_9 orthogonal array by Taguchi optimization method

In this research, four factors were identified namely the intrinsic region length, photo-absorption layer thickness, incident optical power and bias voltage which were tested at three levels using the L_9 orthogonal array by Taguchi optimization method. These factors are portrayed in Fig. 1.

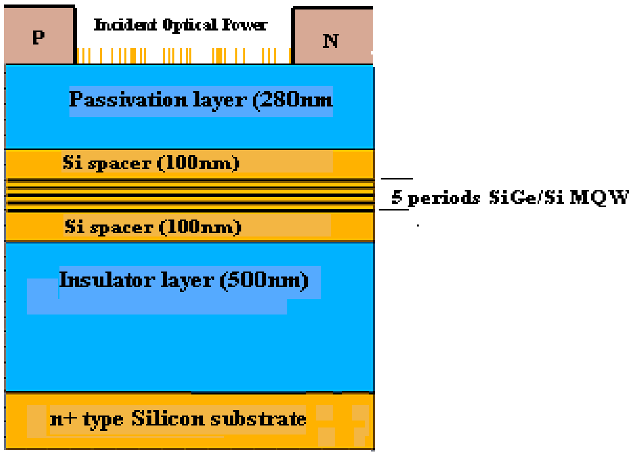

Fig. 1. SiGe MQW device structure.

Whilst, the noise factors were the time and temperature of the n-well diffusion were tested at two levels. By using the S/N ratio and Analysis of Variance (ANOVA) pareto, it allows us to make accurate conclusion for the experiment either the factor is giving dominant effect or minimum effect. To find the optimum factors and levels, signal to noise ratio (SNR) of larger the better (LTB) was applied to examine the performance factors of the device namely the frequency response and the responsivity. The value for the variation was chosen according to previous research. Using L_9orthogonal array method, nine sets of experiments were used to vary the parameter for the intrinsic region length between 6 µm to 8 µm, the photo-absorption layer thickness between 0.305 µm to 0.505 µm, the incident optical power between 0.5 mW/cm^2 to 1.5 mW/cm^2 and the bias voltage between 2.5 V to 3.5 V as shown in Table 1. Then, the parameters of the noise factors for the diffusion time and temperature were tested at two levels which will create four measurements for each row of the L9 orthogonal array.

Table 1. Control factors and their levels.

Set	Parameter	Level			Reference
		1	2	3	
A	Intrinsic region length (μm)	6	7	8	[12]
B	Photo-absorption layer thickness (μm)	0.305	0.405	0.505	[13]-[15]
C	Incident optical power (mW/cm^2)	0.5	1	1.5	[12]
D	Bias voltage (V)	2.5	3	3.5	[16]

The frequency response and responsivity were studied as the output characteristic of the pin-photodiode. Table 2 shows the L_9 orthogonal array to be inserted into Variant 4 factor 3 level.

Table 2. Variant 4 factor 3 level of Taguchi optimization method.

Exp. No.	Control factors			
	A	B	C	D
1	6	0.305	0.5	2.5
2	6	0.405	1	3
3	6	0.505	1.5	3.5
4	7	0.305	1	3.5
5	7	0.405	1.5	2.5
6	7	0.505	0.5	3
7	8	0.305	1.5	3
8	8	0.405	0.5	3.5
9	8	0.505	1	2.5

3. Results and discussion

The simulation results for the responsivity and frequency response of the SiGe/Si MQW SOI-based lateral pin-photodiode is shown in Table 3 and Table 4 respectively. The responsivity and frequency response of the SOI-based lateral pin-photodiode is attributed to SNR of larger-the-better in the Taguchi optimization method. The SNR η can be expressed as:

$$SN = -10\log\frac{1}{n}\left(\sum\frac{1}{y^2}\right) \tag{5}$$

where μ is the mean and σ is the variance. By applying Eq. (5), η for each device was calculated and given in Table 5. The effect of each process parameter on the SNR at different levels can be separated because the experimental design is orthogonal. The SNR values for each level of the process parameters are summarized in Table 6. In addition, the total mean of SNR for these 9 experiments have also been calculated and listed in Table 6.

Table 3. Responsivity values for SOI-based lateral PIN photodiode.

Exp.No.	Responsivity (A/W)			
	1	2	3	4
1	7.85E-01	8.04E-01	8.58E-01	7.94E-01
2	7.19E-01	7.20E-01	7.12E-01	7.19E-01
3	7.90E-01	7.85E-01	7.93E-01	7.84E-01
4	3.78E-01	3.82E-01	3.33E-01	3.72E-01
5	1.18E-02	1.07E-02	1.23E-02	1.41E-02
6	9.38E-01	9.35E-01	9.47E-01	8.90E-01
7	1.58E-01	1.64E-01	1.49E-01	1.58E-01
8	4.33E-01	4.20E-01	4.46E-01	4.41E-01
9	7.90E-02	7.14E-02	6.90E-02	7.08E-02

Table 4. Frequency response values for SOI-based lateral PIN photodiode.

Exp.No.	Frequency response (GHz)			
	1	2	3	4
1	1.10E+10	1.12E+10	1.27E+10	1.28E+10
2	1.33E+10	1.18E+10	1.33E+10	1.17E+10
3	1.28E+10	1.29E+10	1.22E+10	1.28E+10
4	8.48E+09	9.02E+09	8.42E+09	9.08E+09
5	2.27E+09	2.76E+09	4.72E+09	3.31E+09
6	9.93E+09	1.01E+10	9.95E+09	1.02E+10
7	2.18E+09	2.83E+09	2.28E+09	2.18E+09
8	4.45E+09	4.59E+09	3.28E+09	3.20E+09
9	4.28E+09	3.98E+09	4.23E+09	3.61E+09

Table 5. SNR for responsivity and frequency response.

Exp. No.	SNR (dB)	
	Responsivity	Frequency response
1	-1.84	201.46
2	-2.89	201.91
3	-2.07	202.05
4	-8.76	198.83
5	-38.40	189.38
6	-0.66	200.05
7	-16.08	187.33
8	-7.24	191.41
9	-22.82	192.03

Table 6. SNR of the responsivity and frequency response for each level.

Response	Process parameter	SNR (larger-the-best)			Total mean SNR	Maxmin
		Level 1	Level 2	Level 3		
Responsivity	A	-2.27	-15.94	-15.38	-11.19	-13.67
	B	-8.89	-16.17	-8.52		-7.65
	C	-3.25	-11.49	-18.85		-15.6
	D	-21.02	-6.54	-6.02		15.0
Frequency response	A	201.81	196.09	190.26	196.05	11.55
	B	195.87	194.23	198.05		3.82
	C	197.64	197.59	192.92		4.72
	D	194.29	196.43	197.43		3.14

Fig. 2 and Fig. 3 show SNR graphs for the responsivity and frequency response of the SiGe/Si MQW SOI-based lateral PIN photodiode, respectively, where the dashed line is the value of the total mean of SNR. Basically, the larger SNR, the better the quality characteristic for the responsivity and frequency response.

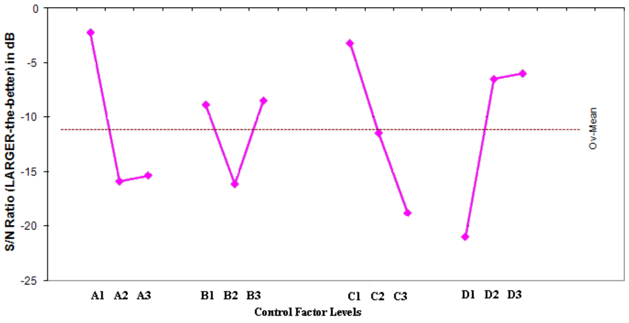

Fig. 2. Signal-to noise ratio graph for responsivity in SOI-based lateral PIN photodiode.

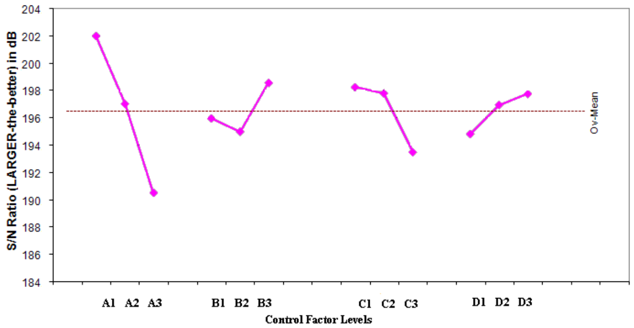

Fig. 3. Signal-to noise ratio graph for frequency response in SOI-based lateral PIN photodiode.

Analysis of Variance (ANOVA)

A better feel for the relative effect of the different process parameter on the responsivity and frequency response were obtained by decomposition of variance, which is called analysis of variance (ANOVA) [17]. The priority of the process parameters with respect to the responsivity and frequency response were investigated to determine more accurately the optimum combinations of the process parameters. The result of ANOVA for the SiGe/Si MQW SOI-based lateral PIN photodiode device is presented in Table 7.

Table 7. Result of ANOVA for responsivity and frequency response in SOI-based lateral PIN photodiode.

Response	Process parameter	Degree of freedom	Sum of square	Mean square	Factor effect on SNR (%)
Responsivity	A	2	359	180	28
	B	2	112	56	9
	C	2	365	183	29
	D	2	435	217	34
Frequency response	A	2	200	100	71
	B	2	22	11	8
	C	2	44	22	16
	D	2	15	8	5

Statistically, ANOVA provides a decision at some confidence level as to whether these estimates are significantly different. The percent factor effect on the SNR indicates the priority of a factor (process parameter) to reduce variation. For a factor with a high percent contribution, it will have a great influence on the performance [18].

For the responsivity characteristic, the bias voltage was found to be the most dominant factor affecting 34% of the device performance, whereas the incident optical power was ranked second (29%). The percentage effect on SNR for the intrinsic region width was the third ranking factor at 28% and the photo-absorption layer thickness is low at 9%. For the frequency response characteristic, the intrinsic region width was found to be the major factor affecting the responsivity (71%), whereas the incident optical power was the second ranking factor of 16%. The percentage effect on SNR for the photo-absorption layer thickness and the bias voltage are low ranking factors at 8% and 5%, respectively. The optimized factors for the responsivity and frequency response in SOI-based lateral PIN photodiode device which was suggested by Taguchi optimization method is shown in Table 8.

Table 8. Best setting of the process parameters.

Response	**Process parameter**	**Unit**	**Best value**
Frequency response & responsivity	Intrinsic region width	(μm)	6
	Photo-absorption layer thickness	(μm)	0.505
	Incident optical power	(mW/cm^2)	0.5
	Bias voltage	(V)	3.5

From the above parameters as shown in Table 8, the final simulation was performed to verify the accuracy of the Taguchi optimization method prediction. In this research, intrinsic region length has the strongest effect on the frequency response characteristics and incident optical power has the strongest effect on the responsivity of the SOI-based lateral PIN photodiode device.

The best result for responsivity after the optimization approaches is 0.87 A/W at the optical wavelength of 1550 nm which is 22.3% better than the previously developed prior to optimization device where the responsivity was 0.71 A/W at 6 μm [9]. Fig. 4 shows the responsivity of the device after optimization.

The best result for frequency response after the optimization approach is 20 GHz. Previously, frequency response of 19 GHz was achieved at an optical wavelength of 1550 nm for a 6 μm intrinsic width of a SOI-based lateral PIN photodiode before prior to optimization [9]. The result is shown in Fig. 5. The measured frequency response for SiGe/Si MQW with absorption thickness of 0.505 μm was higher than that at 0.405 μm. This is due to the fact that the absorption coefficient at 0.505 μm is higher than that at 0.405 μm. Thus, more electron-hole pairs are generated close to the SiGe/Si heterojunction [19].

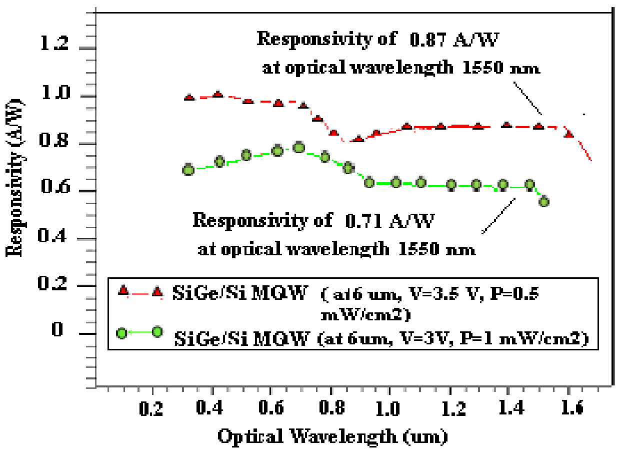

Fig. 4. Responsivity of SiGe/Si MQW SOI-based lateral pin photodiode after optimization.

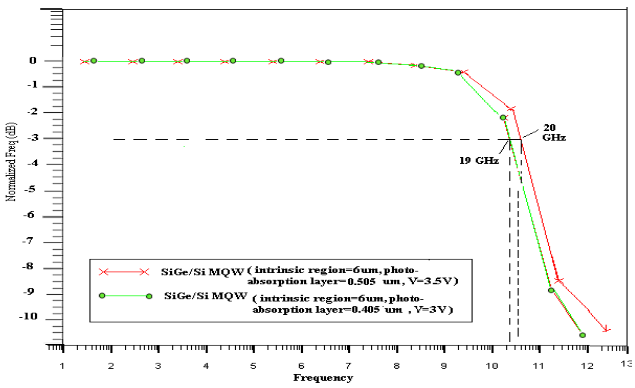

Fig. 5. Frequency response of SiGe/Si MQW SOI-based lateral pin photodiode after optimization.

The transient response for SiGe/Si MQW SOI-based lateral pin photodiode using the best setting after optimization approach is 1.75×10^{-11}s. This result is much better that the result of transient response for the device prior to optimization which is 1.84×10^{-11}s [9]. This is due to the fact that the bias voltage for the device prior to optimization is higher than the device before to optimization. Therefore, the photocurrent is increase in the intrinsic region with high carrier mobility [15]. All photodiode characteristics are affected by change in temperature. There are included the shunt resistance, dark current and other parameters such as junction capacitance [20]. Study the effect of temperature in the next research because it is beyond the scope of research. The summary table for the comparison result of a SiGe/Si MQW SOI-based Lateral PIN Photodiode characteristics between the device after and prior to optimization is shown in Table 9.

Table 9. Summary table.

Characteristics	**After optimization**	**Prior optimization**
Responsivity	0.87 A/W	0.71 A/W
Frequency response	20 GHz	19 GHz
Transient time	1.75×10^{-11} s	1.84×10^{-11} s

4. Conclusion

As a conclusion, the optimum solution in achieving the desired high speed photodiode was successfully predicted using Taguchi optimization method. There are many physical limitations involved as the size gets smaller approaching the molecular or atomic limitations of the substrate and dopant. In this work, Taguchi optimization method was used to optimize the responsivity and frequency response of a SiGe/Si SOI-based lateral PIN photodiode. Therefore, the optical characteristic results of the SOI-based PIN photodiode become better than that of the prior device. The incident optical power and the intrinsic region length were identified as control factors that have the strongest effect on the frequency response and responsivity of the device. Our future work will include the study of device temperature on the responsivity and frequency response because an increase in device temperature will increase the overall noise effects.

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