The electrical characterization of electrodeposited Ni thin film on silicon: Schottky Barrier diodes

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A Ni/n-Si Schottky barrier diode was produced by electrodeposition technique from the electrolyte containing nickel ions under galvanostatic control. The deposition was carried out in a three-electrode cell at room temperature. The electrical characteristics of the Schottky diodes have been investigated using current-voltage (I-V) and capacitance-voltage (C-V) measurements. Ni/n-Si/AuSb diode current-voltage characteristics display low reverse bias leakage currents. The barrier height and ideality factor (n) were obtained 0.60 eV and 3.28 respectively. The high ideality factor value was attributed to oxide layer at the metal semiconductor interface.

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1. Introduction

Magnetic metals and semiconductors play a big role in the present technology. Especially, Schottky Barriers and ohmic contacts produced by combination of rare earth elements (Ni, Co, Fe) with semiconductors are great importance for the device performance such as optical detectors, solar cells [1], chemical sensors [2-3]. Metal-semiconductor (MS) junctions are interested and investigated by science world during recent years. The popularity of such studies rooted in their importance to the insulator layer between metal and semiconductor. The existence of such an insulating layer can have a strong influence on the diode characteristics as well as a change of the interface state charge with bias which will give rise to an additional field in the interfacial layer [4-5]. Therefore, the interfacial layer and the interface states are most important factors in the determination of the barrier height.

The MS surfaces are mostly performed by molecular beam epitaxy (MBE) and sputtering. But these techniques are very costly and require vacuum. The electrodeposition is an alternative way to produce MS surfaces to have Schottky or ohmic contacts. This technique has proven of its simplicity, low cost and the ability of grow metal films from electrolyte. By changing the composition of the electrolyte, it is possible to influence the growth mode and the structure of the deposit.

Here, we report an experimental characterization of the I-V and C-V measurements of MS junction of electrodeposited nickel on n-Si (Ni/n-Si).

2. Experimental

One-sided polished n-Si (111) samples, phosphorus-doped, 1-20 Ωcm (N_D =10^{15}cm^{-3}) were used as substrate. They were cleaned following cleaning procedure [6], which means degreasing in 2-propanol under reflux for 2 h and then boiling alternating for 15 min in basic and acidic H_2O_2 solutions. Prior to each experiment the substrates were etched for 1 min in 20% HF (Merck, VLSI Selectipur) to remove the oxide layer. Ohmic contacts were formed by vacuum evaporation of an Au layer on the back of the wafers after the etching procedure. Subsequently, before electrodeposited Ni, substrates were cleaned with H_2SO_4+H_2O_2+ distilled water (3:1:1) solution to dip for 20 s, rinsed with aceton and a 10:1 buffered HF dip for 1 min, electrodeposition of Ni directly on Si was performed. The role of the HF dip is essential for the fabrication process as it removes the native oxide and prevents its reformation by leaving the Si surface H-terminated [7].

Ni/n-Si Schottky barrier diodes were electrodeposited using a potentiostat/galvanostat with three electrodes, under galvanostatic control. The electrolyte consists of 0.125 M nickel sulphate, 0.25 M boric acid and 0.25 M sodium sulphate. The pH value of freshly prepared electrolytes was 4.0±0.2. A saturated calomel electrode (SCE) and a platinum sheet served as reference and counter electrode, respectively. Film thickness was determined to be 25 μm by deposition time. The current-voltage (I-V) measurements were performed using a Keithley 2400 voltage source and capacitance-voltage measurements were carried out at room temperature with KEITHLEY 590/1M C-V Analyzer. All measurements were controlled by a computer via an IEEE – 488 standard

interfaces so that the data collecting, processing and plotting could be accomplished automatically.

3. Results and discussions

The electrical characterizations were obtained through I-V and C-V measurements at 300 K. The formation of a Schottky barrier between a Ni layer and n-doped Si (111) at room temperature is shown in Fig. 1.

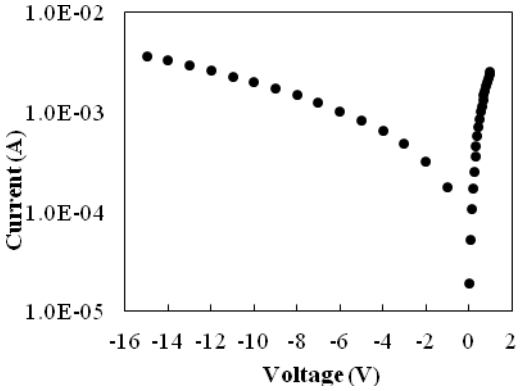

Fig. 1. Experimental forward and reverse bias current versus voltage characteristics in a semilog scale of Ni/ n-Si Schottky barrier diodes at room temperature.

The thermionic emission (TE) theory explains the current flow mechanism across the MS interface in ideal conditions. The current through a Schottky barrier diode at a forward bias *V*, based on the TE theory, is given by the relation [8],

$$J = J_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \qquad (1)$$

where J_0 is the saturation current density is given by

$$J_0 = A^* T^2 \exp\left(-\frac{q\phi_{B0}}{kT}\right) \qquad (2)$$

where *q* is the electron charge, *V* is the forward bias voltage, *k* is the Boltzmann constant, *T* is the absolute temperature, *A* is the effective diode area, $A^* = 4\pi q m^* k^2 / h^3$ is the effective Richardson constant which depends on the effective mass and is equal to 110 A/cm^{2}K^2 for n-type Si, ϕ_{B0} is the zero bias apparent barrier height and *n* is the ideality factor. The saturation current density J_0 was derived by extrapolation of the linear forward part to the axis and it was found to be 1.96x10^{-3} A cm^{-2}, in agreement with the reverse bias current. The ideality factor is a measure of conformity of the diode to pure thermionic emission and is calculated from slope of the linear region of the forward bias $\ln J$ -*V* plot and can be written from Eq.(1) as:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln J)}\right) \qquad (3)$$

The zero-bias barrier height ϕ_{B0} is given by:

$$\phi_{B0} = \frac{kT}{q}\ln\left(\frac{A^* T^2}{J_0}\right) \qquad (4)$$

The semilog-forward bias *I-V* characteristics of the Ni/n-Si(111) Schottky barrier diodes at room temperature is shown in Fig. 2. The experimental values of ϕ_{B0} and *n*, were determined from intercepts and slopes of the forward $\ln J$ versus *V* plot, respectively. The ideality factor and zero bias barrier height of diodes Ni/n-Si were obtained 3.28 and 0.60 ± 0.02 eV, respectively.

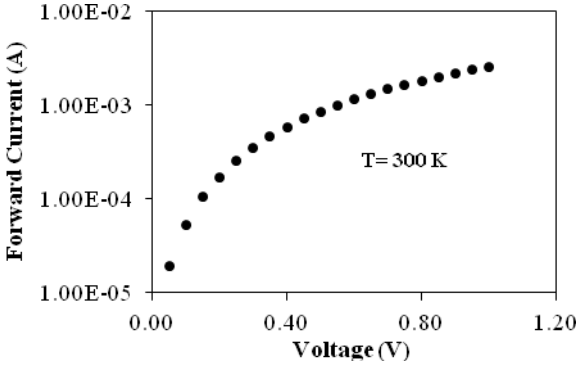

Fig. 2. Semilog forward bias current-voltage (I −V) characteristics of Ni/n-Si Schottky barrier diodes at room temperature.

The bias dependence of the reverse current, often referred to as the soft reverse characteristic, cannot be explained within thermionic emission theory across a sharp barrier using Eq.(1). It may be due to the inhomogeneous Schottky barrier which softens the reverse characteristics significantly [9]. Additionally, tunneling contacts, parellel to the Schottky diode, may be formed on thin oxide layers around the etched window during evaporation.

The capacitance-voltage (C-V) characteristics are one of the fundamental properties of the Schottky barrier diodes structure. Fig. 3 shows the capacitance-voltage characteristics taken at a temperature T=300 K and frequency, f =1 MHz. The characteristics are satisfactorily described by the dependence $C^{-2} \sim V$, typical of a abrupt junction. The gradient of the

$C^{-2} = f(V)$ curve leads to a carrier concentration $N_d = 1{,}9 \times 10^{15}\, cm^{-3}$.

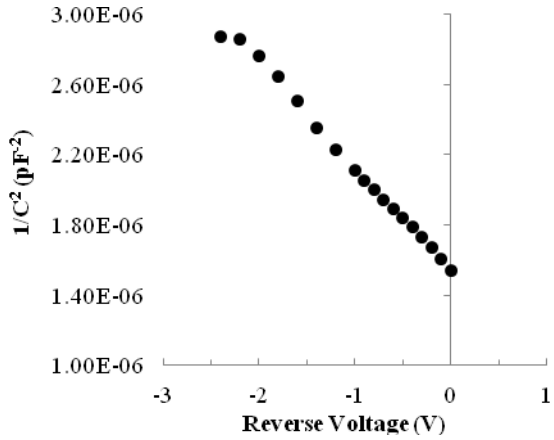

Fig. 3. Capacitance–voltage characteristics of investigated Ni/ n-Si Schottky barrier diodes at room temperature.

At high currents, there is forever a deviation which has been clearly shown to depend on the interface states density and series resistance, associated with bulk material Si and the ohmic back contact, when the applied voltage is sufficiently large. The ideality factor and the series resistance were evaluated using a method developed by Cheung et al. [10]. The Cheung's method is achieved by using the functions;

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + R_S I \tag{5}$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^{*}T^{2}}\right) \tag{6}$$

$$H(I) = IR_S + n\phi_{B0} \tag{7}$$

where ϕ_{B0} is the real barrier height extracted from the lower-voltage part of forward I−V characteristics. The *dV/d(ln(I))* plot is a straight line region where dominates the series resistance. In the plot of *dV/d(ln(I))* versus I , its slope gives the series resistance while its intercept with the *y* - axis gives the ideality factor. The ideality factor is extracted from *dV/ d(ln(I))* plot within voltage range where influence of series resistance is significant. Using so obtained value of ideality factor, the Schottky barrier height is estimated from plot of a function *H(I)* given in Eq.(6). As can be seen from Fig. 4, there is approximately the straight line which intercepts y -axis at the point equal to $n\phi_{B0}$.

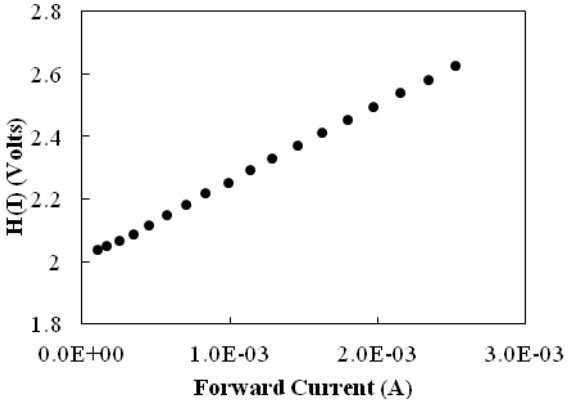

Fig. 4. Experimental H(I) vs. I curve of Ni/n-Si Schottky barrier diodes at room temperature.

4. Conclusions

Electrodeposited Ni / n-Si Schottky Barrier was characterized by I-V and C-V measurements. The basic diode parameters such as ideality factor and barrier height were extracted from these measurements which were carried out at room temperature. It was seen that the barrier height was in good agreement with the literature. High ideality factor value was attributed to oxide layer at the metal semiconductor interface.

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