The electrical properties of nanocluster-CdO/p-type silicon heterojunction structure at room temperature

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The nanocluster CdO thin film was grown on *p*-type silicon substrate by sol-gel method. The structural properties of grown CdO film on Si substrate were investigated by atomic force microscopy (AFM). AFM images indicate that the CdO film is consisted of the clusters formed with coming together of the nano-particles. The heterostructure diode, formed from two semiconductor layers having different optical band gap, *n*-CdO/p-Si is prepared. The electrical properties such as barrier height, ideality factor, interface states density and series resistance of the n-CdO/p-Si heterojunction diode were determined from the current–voltage (*I-V*) measurements. The values of barrier height and series resistance obtained from Cheung and Norde functions of the heterojunction diode were compared with each other. The interface state density (N_{SS}) as a function of energy distribution (E_{SS}- E_V) was extracted from the forward-bias *I–V* measurements by taking into account the bias dependence of the effective barrier height (Φ_b) and series resistance (R_S). The density of the interface state was found to vary from 7.52×10^{12} eV^{-1} cm^{-2} to 5.07×10^{12} eV^{-1} cm^{-2}.

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1. Introduction

The electrical properties of metal–semiconductor (MS), metal–insulator–semiconductor (MIS) Schottky structures have been investigated because of their importance in electronic device applications [1–3]. Semiconductor devices are the basic components of integrated circuits and are responsible for the starting rapid growth of electronics industry in the past fifty years worldwide. Owing to the technological importance of the MS or MIS structures in the electronics industry have been extensively studied both experimental and theoretically [1-10]. As dependent to this situation, in particularly recent years, metal-oxide films such as ZnO, CdO, SnO_2, TiO_2 and etc. that are both transparent in the visible region and electrically conducting, have been extensively investigated due to their potential applications in displays, photo transistors, photovoltaic solar cells, gas sensors, and other optoelectronic devices [4-7]. There are different methods developed on synthesis of CdO films. But, there are a few reports on the synthesis of them using a sol–gel spin coating method [7–10]. The sol–gel method, with the advantage of chemical homogeneity, facility of stoichiometry control, low cost, and also have been applied to deposit CdO film on silicon substrates [11, 12]. Furthermore, the sol-gel spin coating technique has various advantages such as cost effectiveness, thin, transparent multicomponent oxide layers of many compositions on various substrates, simplicity, excellent compositional control, homogeneity and lower crystallization temperature. CdO is an *n*-type semiconductor material with band gap energy between 2.2 and 2.7 eV [13, 14] and the high conductivity of the CdO films results mainly from stoichiometric deviation. Also, cadmium oxide is an inorganic compound with the formula CdO. It is one of the main precursors to other cadmium com- pounds. Therefore, cadmium oxide is considered a promising material for photovoltaic applications due to its high electrical conductivity and optical transmittance in the visible region of solar spectrum [14].

There has been very limited report on Ag/*n*-CdO/*p*-Si MIS structures, especially for that of sol–gel ZnO thin films. Therefore, in this study, CdO film was deposited on silicon by sol–gel method, which is a very simple and economical method. The crystalline structure of the films was studied at room temperature. The electrical properties of the Ag/*n*-CdO/*p*-Si metal-insulator-semiconductor (MIS) structure prepared by sol-gel method have been investigated by means of current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements. Electronic properties of Ag/*n*-CdO/*p*-Si diode were characterized by its main electrical parameters such as ideality factor, barrier height, series resistance and interface states

parameters. The barrier height and series resistance obtained from Cheung [15] functions was compared with those from Norde's [16] function. Furthermore, the energy distribution (E_{SS}- E_V) of interface state densities (N_{SS}) obtained from the forward-bias *I–V* characteristics of the Ag/*n*-CdO/*p*-Si (MIS) structure at room temperature. The experimental results show that the series resistance value should be taken into account in determining the interface-state density distribution curves.

2. Experimental details

The cadmium oxide thin film was prepared using cadmium acetate dehydrate ($Cd(CH_3COO)_2{\cdot}2H_2O$), 2-metoxyethanol and ethanolamine. For this, 0.5 M of cadmium acetate dehydrate ($Cd(CH_3COO)_2{\cdot}2H_2O$) was firstly dissolved in 2-metoxyethanol for 2 h at room temperature and then, ethanolamine was added to this solution. The solution was stirred using magnetic stirrer for about 30 min to obtain clear homogeneous solution and then sol was kept for aging for 24 h prior to film deposition. *p*-type single crystal silicon with a thickness of 600 μm, and a resistivity of 5–10 Ω–cm was used for fabrication of the diode. Firstly, p-type single crystal silicon was cleaned. In order to remove the native oxide on surface of p-Si, the wafer was etched by HF and then it was rinsed in deionised water using an ultrasonic bath for 10–15 min and finally was chemically cleaned according to method based on successive baths of methanol and acetone. The ohmic contact was formed by evaporating Al metal on the back of Si wafer and then, it was annealed at 570 °C for 3 min in N_2 atmosphere. Afterwards, CdO film was deposited on p-type-silicon using a spin coating coater with 2000 rpm and then, the film was dried at 150 °C for 10 min onto a hot plate to evaporate the solvent and remove organic residuals. The prepared CdO film was annealed at 450 °C for 1 h in a furnace. The thickness of the CdO film was determined to be 187 nm using atomic force microscopy. The Ag top electrode contact of the diode was using PVD-HANDY/2S-TE (Vaksis Company) vacuum thermal evaporation in the pressure of 4.5×10^{-5} Torr and the contacts were formed in the form of circular dots of 2 mm in diameter and 100 nm thicknesses. The contact area of the diode was found to be 3.14×10^{-2} cm^2. The cross-section of Ag/*n*-CdO/*p*-Si/Al diode is shown in Fig. 1. The current–voltage and capacitance-voltage characteristics of the Ag/n-CdO/p-Si MIS diodes were performed using a KEITHLEY 4200 Semiconductor Characterization system. The structural properties of the CdO film was investigated by PARK system XE100E atomic force microscopy.

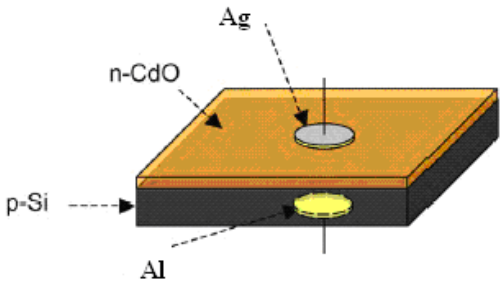
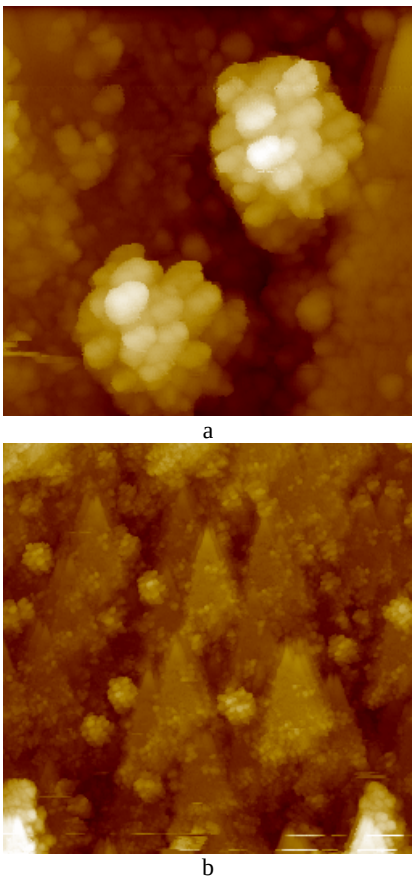


Fig. 1. The schematic diagram of the Ag/n-CdO/p-Si MIS structure.

3. Results and discussion

Fig. 2 (a and b) shows atomic force microscopy (AFM) images of the CdO film deposited on p-type Silicon substrate at two different magnifications. Fig. 2 a, the clusters which homogenously spread on the whole of the film surface are seen. Also, as seen in Fig. 2 b, the clusters are formed from the nanoparticles. The nature and distribution of microstructures suggest the accumulation of grains in some positions and then inhomogeneous distribution of CdO particles throughout the surface of the p-Si substrate. The diameter of the clusters is approximately 300–350 nm. The clusters are consisted of nano-particles of about 70–90 nm.



a

b

Fig. 2 (a, b). Atomic force microscopy (AFM) image of the Ag/n-CdO/p-Si structure.

The current–voltage characteristics of the *n*-CdO/*p*-Si heterojunction diode are shown in Fig. 3. At lower voltages, the current passing through the diode increases exponentially with increasing voltages. This suggests that the current–voltage characteristics of the Ag/*n*-CdO/*p*-Si diode can be analyzed by the thermionic emission (TE) theory [16-18];

$$I = I_o \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

where I_0 is the reverse saturation current given by

$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_{bo}}{kT}\right) \quad (2)$$

where A is the diode area (3.14×10^{-2} cm^2), A^* is the effective Richardson constant (32 Acm^{-2} K^{-2} for p-Si) Si [17-18], V is the applied voltage drop across the junction, q is the electronic charge, k is Boltzmann's constant, T is the absolute temperature, Φ_{bo} is the zero-bias barrier height, and n is the diode ideality factor which is a measure of conformity of the diode to pure thermionic emission. The ideality factor of the diode was determined from the slope of the linear region of forward bias of Fig. 3 and was found to be 8.40. The barrier height of the diode was calculated using the reverse saturation I_o value obtained from Fig. 3 and was found to be 0.66 eV. The higher value of ideality factor of the Ag/*n*-CdO/*p*-Si diode is attributed to the interface states and series resistance effects which cause the non-ideal behaviour. Thus, the series resistance effect cannot be ignored. The effect of series resistance can be analyzed by Cheung and Norde's method defined by the following relations;

$$\frac{dV}{d(\ln I)} = R_s I + n\frac{kT}{q} \quad (3)$$

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \quad (4)$$

and

$$H(I) = IR_S + n\Phi_{bo} \quad (5)$$

Figure 3

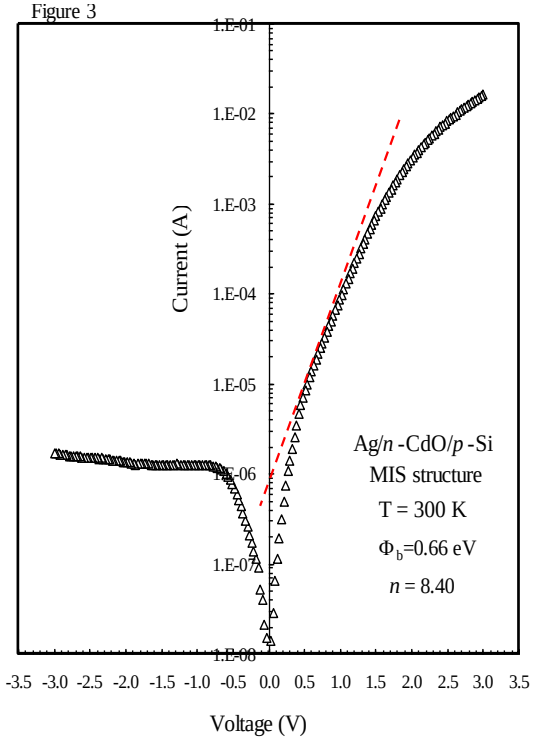


Fig. 3. Forward and reverse bias current-voltage plot of the Ag/n-CdO/p-Si MIS structure.

Eq. (3) should gives a straight line for the data of downward curvature region of the forward bias *I-V* characteristics. Therefore, the slope and y-axis intercept of a plot of $dV/d\ln(I)$ versus I will give R_S and nkT/q, respectively. Fig. 4 shows the plot of $dV/d\ln(I)$ vs. I at room temperature. The parameter R_S is effective in the non linear region of the forward *I–V* characteristics in Fig. 3. The series resistance effect corresponds clearly to the current range of 1×10^{-3}– 1×10^{-2} A, as shown in Fig. 3. From Fig. 4 (a), the values of n and R_S have been calculated as n=11.91 and R_S = 38.67 Ω from the linear region of the plot of $dV/d(\ln I)$ vs. I, respectively. It is observed that there is a large difference between the value of n obtained from the forward bias *lnI–V* plot and obtained from the $dV/d(lnI)$–I curve. This may be attributed to the existence of the series resistance and the interface states and to the voltage drop across the interfacial layer [17-20]. Furthermore, according to Cheung's method (From Fig. 4 (b)), $H(I)$ vs. I plot has to be linear according to Ref. [15]. The slope of this plot gives a different determination of R_S. By using the value of n obtained from Eq.(3), a plot of $H(I)$ versus I according to Eq. (5) will also give a straight line with y-axis intercept equal to $n\Phi_b$. The values of R_S and Φ_b were obtained to be 38.19 Ω and 0.602 eV from *H(I)-I* plot, respectively. As shown in Fig. 4, the values of series resistance obtained from Cheung functions are equal with each other. Besides, Norde proposed an alternative method to determine the value of the series resistance and barrier height. The following function is defined for modified Norde method [16]:

$$F(V)=\frac{V}{\gamma}-\frac{kT}{q}\ln\left(\frac{I(V)}{AA^{*}T^{2}}\right) \quad (6)$$

where γ is an arbitrary integer greater than *n* (γ >*n*). *I*(*V*) is the current obtained from the *I–V* curve. Once the minimum of the *F(V)* versus *V* plot is determined, the value of barrier height (Φ_b) can be obtained from Eq.(6). Thus, from Norde's functions, the barrier height and series resistance values of the diode are calculated by the following relations:

$$\Phi_b = F(V_0)+\frac{V_0}{\gamma}-\frac{kT}{q} \quad (7)$$

$$R_S = \frac{\gamma-n}{I}\quad\frac{kT}{q} \quad (8)$$

Where, $F(V_0)$ is the minimum point of $F(V)$, and V_0 is the corresponding voltage. Fig. 5 shows the $F(V)$–V plot of the heterojunction diode. Using Eq. (7) and Eq. (8), the barrier height Φ_b and series resistance R_S values for the diode were found to be 0.77 eV and 82.28 Ω, respectively. There is a difference among the values obtained from the forward bias *lnI–V*, Cheung functions and Norde functions. Differences in among the values obtained from three methods for the device may be attributed to the extraction from different regions of the *I-V* curve [20,21]. The value of the series resistance obtained from Cheung functions is smaller than that obtained from Norde function. Norde's functions are applied to the full forward bias region of the ln*I–V* characteristics of the junctions, while Cheung functions are only applied to the nonlinear region in high voltage region of the forward bias *I–V* characteristics [16, 20, and 21]. Also, the series resistance value obtained from Norde functions can be much higher than that of Cheung model for especially non-ideal rectifying structures.

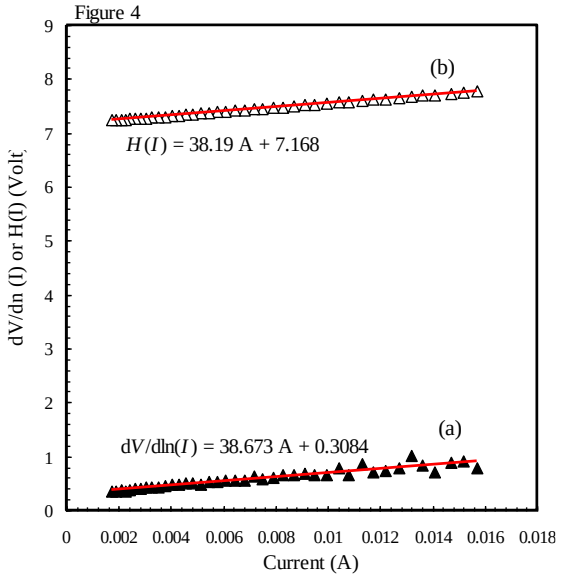


Fig. 4. The experimental H(I) vs. I and dV/dln(I) vs. I plots of the Ag/n-CdO/p-Si MIS structure.

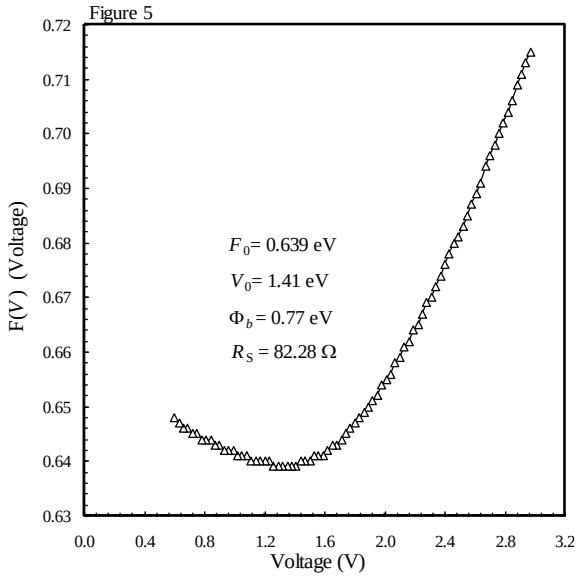


Fig. 5. F(V) vs.V plot obtained from forward bias current-voltage characteristics of the Ag/n-CdO/p-Si MIS structure.

The capacitance-voltage characteristic is one of the fundamental properties of metal–semiconductor (MS) or metal–insulator–semiconductor (MIS) Schottky structures, and capacitance-voltage measurements can provide valuable information about the fixed charge concentration and the barrier height. Thus, another often used and convenient technique to measure the SBH **is** the C–V technique. Figs. 6 (a and b) show the *C–V* and C^{-2}-*V* characteristics at room temperature measured at frequency of 500 kHz, respectively. As can be seen in Fig. 6a, the zero-bias capacitance is seen step from 3.77×10^{-9} pF, due to oxide layer. The C^{-2}–*V* characteristic illustrated in Fig. 6 (b) is linear in the between -3.0 V and 0 V at 500 kHz. The depletion layer capacitance of the diode can be expressed as;

$$\frac{1}{C^2}=\frac{2(V_R+V_a)}{q\varepsilon_S N_A A^2} \quad (9)$$

The slope of the reverse bias C^{-2}-*V* plot can be also given by:

$$\frac{d(C^{-2})}{dV}=\frac{2}{N_A A^2 q\varepsilon_S} \quad (10)$$

where A, is the area of the diode, V_R the reverse bias voltage, V_a is diffusion potential at zero bias and is determined from the extrapolation of the C^{-2}-*V* plot to the *V*-axis, ε_s is the dielectric constant of the Si (=11.8εo), *q* is the electronic charge and N_A is the carrier concentration. The diffusion potential or built-in potential is usually measured by extrapolating C^{-2}-*V* plot to the *V*-axis. The barrier height, Φ_{CV}, from *C-V* measurement is defined by;

$$\Phi_{CV}=qV_a+E_F-\Delta\Phi_b \quad (11)$$

where $\Delta\Phi_b = \sqrt{qE_m/4\pi\varepsilon_s\varepsilon_0}$ is the image force alone causes barrier lowering, $E_m = \sqrt{2qN_A V_D/\varepsilon_s\varepsilon_o}$ is the maximum electric field, V_a is the intercept point of V axis from C^{-2}-V curve, and E_F, $E_F = kT\ln\left(\frac{N_V}{N_A}\right)$, is the potential difference between the Fermi level and the top of the valance band in the neutral region of p-Si and can be calculated knowing the carrier concentration N_A and the effective density of states in the valence band. According to Eq. (11), the barrier height $\Phi_b(C\text{-}V)$ was found to be 0.88 eV and the carrier concentration was determined to be 2.47×10^{15} cm^{-3}. Due to different nature of the C–V and I–V measurement techniques, the barrier heights deduced from them are not always the same. It is seen that, on the contrary literature, the $\Phi_b(C\text{-}V)$ value obtained from C–V measurement is smaller than that of Φ_b value obtained I–V measurements.

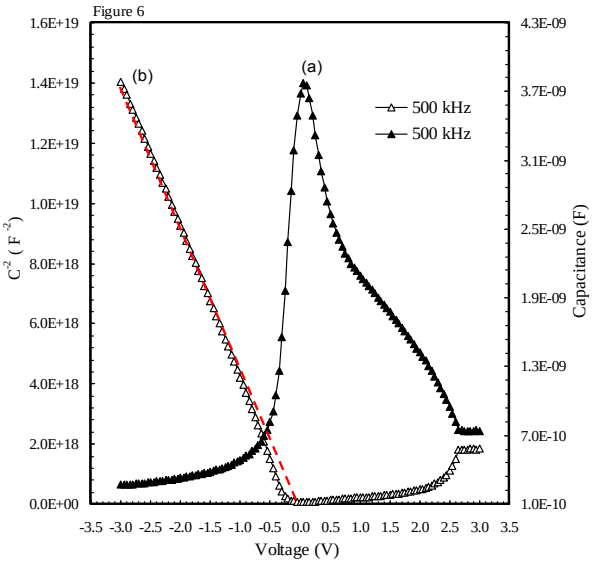


Fig. 6. (a) The experimental capacitance-voltage and (b) reverse bias C^{-2}-V characteristics of the Ag/n-CdO/p-Si MIS structure at a frequency 500 kHz.

The most important characteristics of the MS or MIS interface are the nature of the potential barrier between the Fermi level in the metal and the majority carrier's band edge of the semiconductor at that interface. The interface states (N_{SS}) as dependence to energy distribution (E_{SS}-E_V) of the Ag/n-CdO/p-Si MIS structures is given in Fig. 7. As seen in Fig. 7, the interface state density has an exponential drop with bias from the midgap towards the top of the valance conduction band for Ag/n-CdO/p-Si MIS structures. For an MS diode having interface states in equilibrium with the semiconductor, the ideality factor n becomes greater than unity as proposed by Card and Rhoderick [22] and then the interface-state density N_{SS} is given by;

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_s}{W_D}\right] \quad (12)$$

where W_D is the space charge width ($W_D = 4150\ ^oA$), N_{SS} is the density of interface states, ε_s and ε_i are the permittivity of the semiconductor and oxide layer, respectively, and δ is the thickness of oxide layer, and $n(V)=V/(kT/q)\ln(I/I_0)$ the voltage-dependent ideality factor. Also, in p-type semiconductors, the energy of the interface states, E_{SS}, with respect to the top of the valance band, E_V, at the surface of the semiconductor is given by [17,18, and 23];

$$E_{SS} - E_V = q(\Phi_e - V) \quad (13)$$

where V is the applied voltage drop across the depletion layer and Φe is the effective barrier height. Thus, we can use Eq. (13) together with Eq. (12) in the calculation of the interface state density distribution. As can be seen in Fig.3, the forward bias I–V characteristics are linear in the semi-logarithmic scale at low voltages, but deviate considerably from linearity due to the effect of parameters such as the series resistance and the interface states when the applied voltage is sufficiently large. Thus, as seen in Fig. 7, these values of N_{SS} were converted to a function of (E_{SS} −E_V) using Eq. (13), and N_{SS} increases exponentially with bias from 5.07×10^{12} cm^{-2}eV^{-1} to 7.52×10^{12} cm^{-2}eV^{-1} eV. It is evaluated that the role of nanoclusters in transport phenomena as nanoparticles will introduce the energy levels in band gap of the material and results in the increase the interface state density at the interface. This case may be ascribed to the chemical reactivity of Schottky metal. That is, chemical reactions involving oxygen could also change the distribution of states at the interface [24, 25]. Almost all metals react with silicon at some temperature forming a wide variety of silicides or alloys. Such reactions can be initiated even during room-temperature deposition of the metals and extend generally over at least a few monolayer [25].

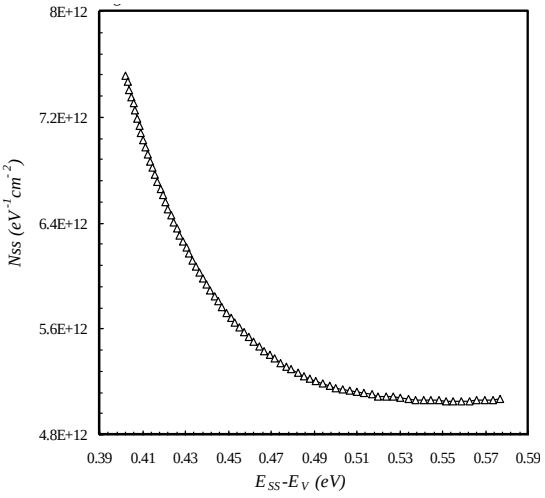


Fig. 7. The interface state energy distribution curves of the Ag/n-CdO/p-Si MIS structure obtained from I-V measurements.

4. Conclusions

Electrical characteristics of the Ag/*n*-CdO/*p*-Si diode were analyzed using *I–V* and *C–V* measurements. The structural properties of the CdO film were investigated. The AFM images indicate that the surface of the CdO film is consisted of the clusters formed with the coming together of the nano-particles. The main parameters such as barrier height, ideality factor, interface states density and series resistance of the Ag/*n*-CdO/*p*-Si diode were determined from the current–voltage measurements. The obtained n value of 8.40 suggests that the diode exhibits a non-ideal behaviour. This behaviour results from the presence of surface states in CdO, oxide layer on silicon and series resistance. The interface state density N_{ss} obtained from the forward bias *I–V* ranges from 5.07×10^{12} $cm^{-2}eV^{-1}$ to 7.52×10^{12} $cm^{-2}eV^{-1}$ eV.

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