

Tri-state switching behavior in a GaAs/InGaAs barrier structure

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In this study, a new GaAs/InGaAs potential barrier switching device combined with a p-n hole injector is fabricated and demonstrated. Two GaAs/InGaAs barriers are employed to provide potential barriers for electron thermionic emission and hole confinement. While applying a sufficient bias voltage to this device, a double S-shaped negative differential resistance (NDR) phenomenon with nearly equal switching voltage difference is appeared at room temperature. This unique NDR property can be introduced to triple stable regions into the device circuit design. Based on a proper circuit design with suitable load line, the studied device has potential for tri-state logic applications.

(Received October 15, 2011; accepted November 23, 2011)

Keywords: Thermionic emission, Hole confinement, Negative differential resistance (NDR), Triangular barrier (TB), Tri-state

1. Introduction

Several kinds of negative differential resistance devices have been studied to date [1-4], especially the devices with S-shaped NDR are very attractive. Among them devices such as the pnpn thyristor structure [1-2] and p⁺-n-i- δ (p⁺)-i-n-n⁺ triangular barrier structure [3] has been broadly studied. The former utilizes the avalanche multiplication process in the reverse-biased region for switching, but the latter device changes the state by the internal barrier collapse due to the hole confinement. Thus, the S-shaped NDR in the triangular barrier structure is mainly attributed to the internal barrier collapse dominated by the hole injection from the pn junction. The accumulated holes at the barrier potential minimum effectively lower the barrier height, which also increases the thermionic electrons over the barrier at the conduction band. Through a series of barrier lowering, the positive feedback phenomenon is finally established. A large current flow makes the device change state from a high-impedance off-state to a low-impedance on-state [5]. During the device growth in the delta-doped layer, the high quality MOCVD and MBE techniques have been successfully developed and applied to prepare nano-scale structures [6-7].

In this paper, a novel asymmetric TB switch is grown by MOCVD, and demonstrates an interesting sequential double S-shaped NDR behaviors. Based on the idea of modulating the different barrier height, a conceptual

understanding of experimental results would enhance our understanding of the operation of TB-like switching devices. To our knowledge, this is the first demonstration of double S-shaped NDR using GaAs/InGaAs triangular potential barriers. Detailed investigation of sequential switching behavior using GaAs/InGaAs barriers is still limited.

2. Experimental

The cross-section view of a GaAs/InGaAs TB switch is schematically shown in Fig. 1. The studied films were grown by the MOCVD system [8] on a (100)-oriented Si-doped GaAs substrate. The epitaxial layers were grown on a substrate at 850 °C with a growth rate about 0.8 um/hr. Precursor sources were stored in bubblers located in a gas mixing cabinet. Trimethylgallium (TMGa), trimethylindium (TMIn) and arsine (AsH₃) were used as material sources where the hydrogen was acted as the carrier gas. The device structure consists of a 0.4 um n-GaAs ($1 \times 10^{17} \text{cm}^{-3}$) buffer layer, a delta-p⁺ GaAs ($5 \times 10^{18} \text{cm}^{-3}$) sandwiched by two 5 nm In_{0.2}Ga_{0.8}As layers, a 1.0 um n-GaAs ($5 \times 10^{16} \text{cm}^{-3}$) transition layer, a delta-p⁺ GaAs ($5 \times 10^{18} \text{cm}^{-3}$), a 0.4 um n-GaAs ($1 \times 10^{17} \text{cm}^{-3}$), and a 0.2um p⁺-GaAs ($1 \times 10^{18} \text{cm}^{-3}$) cap layer acted as the hole injector.

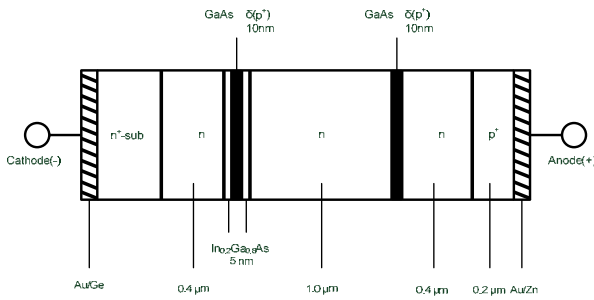


Fig. 1. The cross-section view of a GaAs/InGaAs TB switch.

After finishing the film growth and photolithography process, the device isolation mesa was processed by employing the $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ chemical etching solution to form $150 \mu\text{m} \times 150 \mu\text{m}$ mesa islands. Au/Zn was thermal evaporated as ohmic contact for the p type anode metal by lift-off technique. All the I-V switching characteristics were measured in the dark using probe station and Aglient E5263 I-V curve tracer.

3. Results and discussion

The operation principle of the double S-shaped switching device can be explained by the band diagram. Fig. 2(a) illustrates the band diagram at thermal equilibrium, in which exists two different GaAs/InGaAs internal barriers. There are two triangular barriers with different barrier height, denoted as B_1 and B_2 , in the n-layer region, respectively. Considering the bias condition depicted in Fig. 1, the anode is positively biased relative to the cathode, this confirms the switching behavior. In Fig. 2(a), while applying a small voltage at double TB heights, it is sufficiently difficult to overcome for electrons to thermionic emission across the internal barrier, which introduces the high-impedance off-state. At this condition, this device acts like a TB diode, in which the current are exponentially increased with increasing external voltage [9]. But, if the applied voltage V_{AK} is increased up to the first switching voltage (V_{S1}), the increased number of accumulated holes also in the potential minimum of B_1 , resulting from the forward p⁺-n junction, are sufficient to lower the effective barrier height of B_1 . Therefore, some electrons can be thermionic over the barriers due to the decrease of the barrier height of B_1 , resulting in a small conducting current. The corresponding band diagram at the beginning of the first switching is shown in Fig. 2(b). When the barrier of B_1 is completely collapsed, the device is transferred from the high-impedance off-state into the medium-impedance quasi on-state. Then, the applied voltage is almost biased across the bottom InGaAs barrier of B_2 . As further increasing the applied voltage, V_{AK} , up to the second switching voltage, V_{S2} , holes drifting from the potential minimum of B_1 to B_2 , will greatly increase the number of holes in the potential minimum of B_2 . This, in turn, yields a significant probability of thermionically

emitted electrons over the B_2 barrier, resulting in the lowering of B_2 and a higher conducting current. The corresponding band diagram is shown in Fig. 2(c). As described above, a positive feedback will be established while the potential-barrier heights of B_1 and B_2 are finally lowered, as illustrated in Fig. 2(d). Consequently, the device is transferred from the quasi on-state into the final low-impedance on-state. The conducting current dramatically increases with increasing the applied voltage. The final holding voltage is dependent on the voltage drops on the two internal barriers.

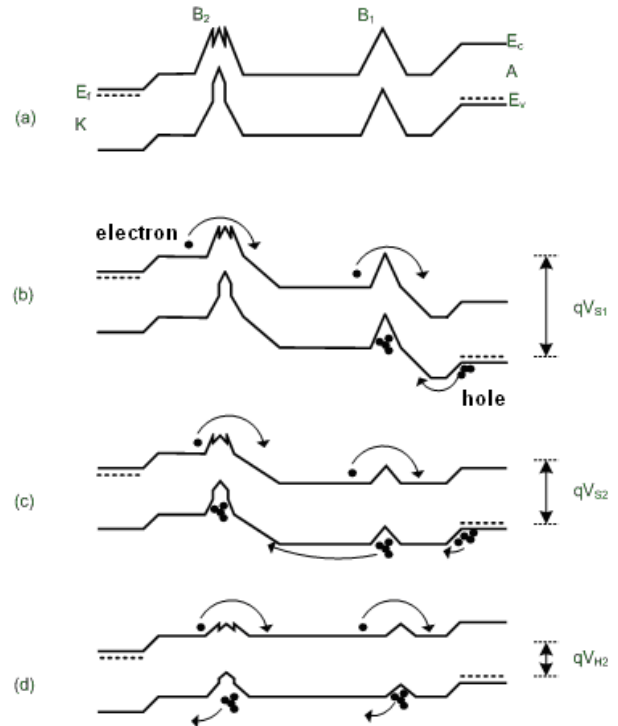


Fig. 2. Energy band diagrams of the studied switching device at (a) thermal equilibrium (b) the beginning of the first initial switching (c) the beginning of the second initial switching (d) the final on-state holding voltage.

Fig. 3 shows the I-V characteristics of the device measured at room temperature. A significant double S-shaped NDR characteristic is clearly observed. The measured switching and holding voltages of the first and second switching behaviors are $V_{S1} = 5.5\text{V}$ (point a), $V_{H1} = 4.2\text{V}$ (point b) and $V_{S2} = 3.6\text{V}$ (point c), $V_{H2} = 1.8\text{V}$ (point d), respectively. It is worth noting that the voltage difference (1.3V) between V_{S1} and V_{H1} is not equal to the difference (1.8V) between V_{S2} and V_{H2} . According to the band diagrams described above, the difference is due to the barrier lowering of B_1 and B_2 . Since the barrier heights used for either B_1 or B_2 are not the same in the device, thus both of the barrier lowering is expected to be not equal. The final holding voltage ($V_{H2} = 1.8\text{V}$) is nearly across at

the voltage drops resulted from the collapse of two internal GaAs/InGaAs barriers. From experiment, it is also found that the device current is exponentially increased at the small current range (curve o→a). Its I-V characteristic can be transferred into $\log I$ versus V , which is also depicted in the inset of Fig. 3. As we know, the diode ideal factor (n) and barrier height (Φ_b) are given by

$$n = \frac{1}{V_T} \frac{\partial V}{\partial \ln I}$$

$$\phi_b = V_T \ln \left(\frac{AA^* T^2}{I_s} \right)$$

where A^* , A , V_T are the Richardson constant, device area and thermal voltage, respectively.

From experiment, the calculated ideal factor (n) and barrier height (Φ_b) are 2.18 and 0.68 eV, respectively.

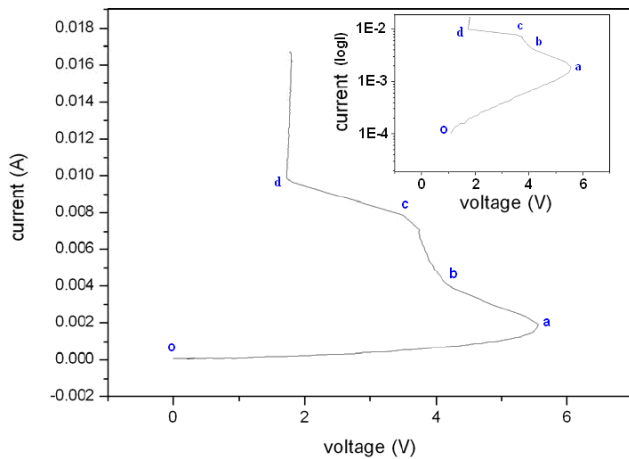


Fig. 3. Double S-shaped switching I-V characteristics of the studied device at room temperature. The $\log I$ versus V characteristic is also shown in the inset.

Fig. 4 shows the schematically typical I-V characteristics of the studied device and the circuit design. The switching sequence can be illustrated as 1 → 2 → 3 → 4 → 5 → 6 with increasing V_{AK} external voltage. Owing to the unique double S-shaped I-V behavior, this device may be employed for tri-state logic circuit applications [10]. Under a DC supply voltage, V_{SS} , and a load resistor, R_L , the load line intersects the I-V curves at three stable points, that is, Q_0 , Q_1 and Q_2 . The output voltages V_0 , V_1 and V_2 are then corresponding to the output logic levels 0, 1 and 2, which are also shown in the inset of Fig. 4. If a short pulse is now employed in the circuit, the circuit operation can be switched from one stable state to other states. By introducing a load resistor $R_L = 250 \Omega$ and an external DC voltage $V_{SS} = 6 \text{ V}$, the load line intersects at voltages $V_0 = 5.2 \text{ V}$, $V_1 = 3.8 \text{ V}$ and $V_2 = 2.0 \text{ V}$, which represent the output logic levels 0, 1 and 2,

respectively. In this device circuit, it is found that the voltage difference of output levels is very close due to the nearly symmetric double switching behavior. Hence, this switching device may have good potential for triple-valued logic circuits with an improved device structure. Applications for such a new switching device are under development.

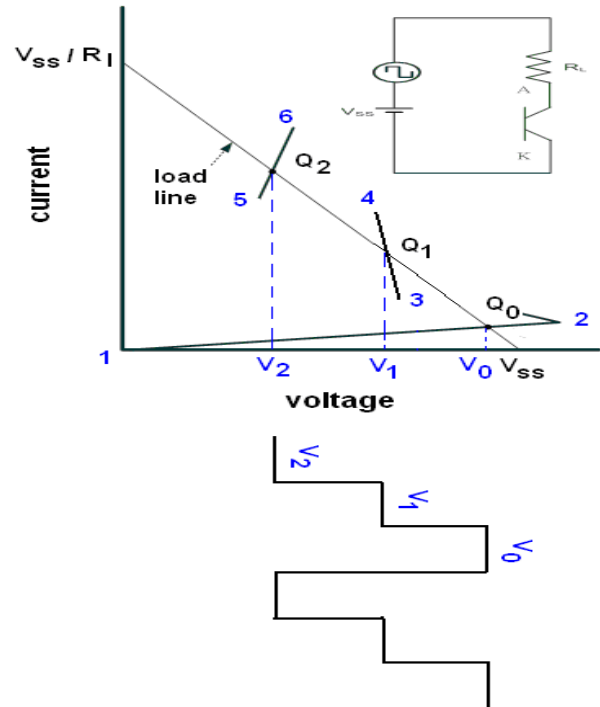


Fig. 4. Schematic I-V characteristic of the tri-state switch and its bias circuit. The tri-state operation output can be expected as V_0 , V_1 and V_2 , respectively.

4. Summary

Using the hole confinement effect of different GaAs/InGaAs triangular barriers, a triple state switching device has been developed. An interesting double S-shaped NDR and nearly symmetric switching voltage difference appear in the I-V characteristics. The transport mechanism of the unique double switching phenomenon at the room temperature has been analyzed with the energy band diagrams. From two sequential collapses of GaAs/InGaAs internal barriers, the double NDR characteristic is achieved. This device may show good potentials for switching device and triple-valued logic applications.

References

- [1] G. W. Taylor, J. G. Simmons, A. Y. Cho, R. S. Mand, *J. Appl. Phys.* **59**, 596 (1986).
- [2] K. Kasahara, Y. Tashiro, N. Hamao, M. Sugimoto,

- T. Yanase, *Appl. Phys. Lett.* **52**, 679 (1988).
- [3] C. Amano, S. Matsuo, T. Kurokawa, *IEEE Photon. Technol. Lett.* **3**, 736 (1991).
- [4] Y. Kawamura, H. Asai, S. Matsuo, C. Amano, *IEEE J. Quantum Electron.* **QE-28**, 308 (1992).
- [5] K. F. Yarn, Y. H. Wang, C. Y. Chang, *J. Appl. Phys.* **5**, 2695 (1994).
- [6] E. F. Schubert, Y. Horikoshi, K. Ploog, *Phys. Rev. B* **32**, 1085 (1988).
- [7] K. Ploog, M. Hauser, A. Fischer, *Appl. Phys. A* **45**, 233 (1988).
- [8] C. I. Liao, K. F. Yarn, C. L. Lin, Y. H. Wang, *Jpn. J. Appl. Phys.* **41**, 1247 (2002).
- [9] S. E. D. Habib, K. Board, *IEE Proc. I*, **130**, 292 (1983).
- [10] K. F. Yarn, Y. H. Wang, M. S. Chen, *Mater. Sci. Eng. B-35*, 29 (1995).

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